TB-7VX-690T/980T/1140T-PCIEXP Hardware User's Manual

Rev.1.04

Revision History

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Rev.1.02	2014/0318	Modified worng informations	Yoshioka
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Introduction

Thank you for purchasing the **TB-7VX-690T/980T/1140T-PCIEXP** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	If an unpleasant smell or smoking occurs, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	Do not disassemble, repair or modify the product. Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	Do not touch a cooling fan. As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	Do not place the product on unstable locations. Otherwise, it may drop or fall, resulting in injury to persons or failure.
	If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.
	Do not touch the product with a metallic object. Otherwise, a fire or electric shock may occur.
	Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.
	Do not get the product wet or touch it with a wet hand. Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	Do not touch a connector on the product (gold-plated portion). Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
⃠	**Do not use or place the product in the following locations.** • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
⃠	**Do not place heavy things on the product.** Otherwise, the product may be damaged.

■ Disclaimer

This product is an evaluation board for Xilinx Virtex-7 FPGA. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Board Accessories

Related documents:
All documents relating to this board can be downloaded from our website. Please refer to attached paper of the products.

Board Fixer:
Fan/heat sink set (Fan: 1, Heat sink: 1, M3 X 20 screw: 2, Washer: 2)
XH connector (JST: B3B-XH-A): 1
DDR3-SO-DIMM: 4G byte x2

Board Accessories:
Board foot set (Rubber foot: 7, M3 X 6 screw: 14, M3 X 10 spacer: 7)
AC/DC power supply (12V/15A): 1
AC power supply cable with a power switch: 1
DC power supply cable: 1
microSD card for FPGA Configuration (2G byte): 1

2. Overview

This board is the high-speed and high-density PCI Express Gen3 evaluation board equipped with Xilinx Virtex7 Series FPGA "XC7VX690T/980T-2FFG1926 or 1140T-2FLG1926".

3. Feature

- PCI Express Gen3(x8) interface
- High-Pin Count FMC connector x 4
  - Due to limitation of the number of FPGA pins, all the defined FMC connector pins are not connected. For more information, refer to the corresponding connector pinout table contained in this document.
  - FMC4 has a limitation of GTH usage. For more detail, please refer to section 7.3.4
- DDR3 SO-DIMM: 4GB x 2
- QSPI Flash for user application
- USB 3.0 device connector
- PMOD connector
- Various clock sources
- For operation: PushSWs, DipSWs, PinHeaders
- For monitoring: LEDs
- Configuration from microSD Card(Spartan3 FPGA is configuration controller)
- Configuration from BPI Flash(Spartan3 FPGA is configuration controller)
- JTAG interface to Virtex-7 FPGA directly.

4. Block Diagram

The following figure shows the block diagram of this board.

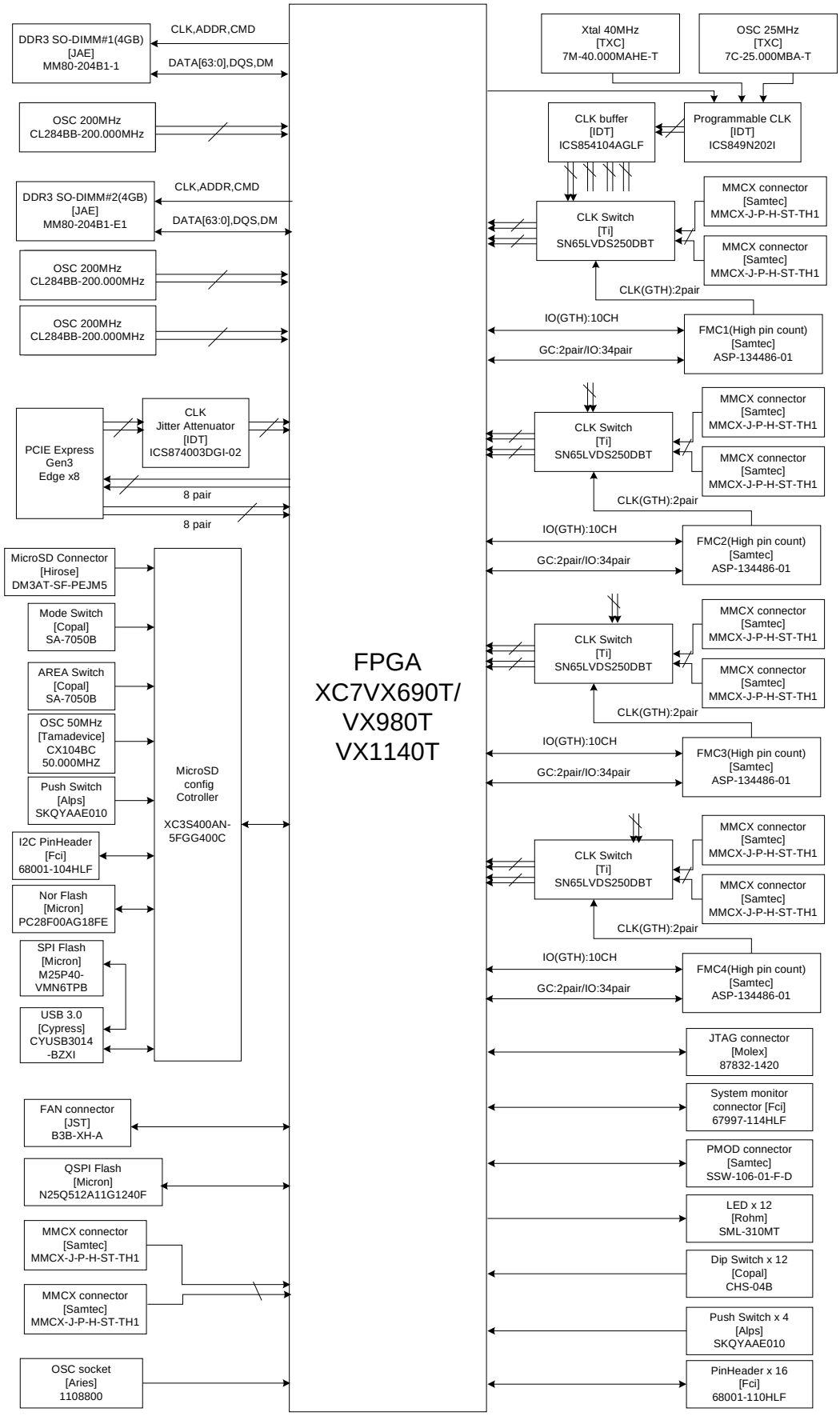

Figure 4-1 Block Diagram

5. External View of the Board

The following figures show the external views of the board.

Figure 5-1 Component Side of the Board

6. Board Specification

External Dimensions:	W:312mm x H:130mm (non-compliance with PCI-Express specification)
Number of Layers:	16 Layers
Board Thickness:	1.7 mm
Material:	FR-5
FPGA:	Xilinx XC7VX690T/980T-2FFG1926, XC7VX1140T-2FLG1926
BPI-FLASH:	Micron PC28F00AG 18FE
QSPI-FLASH:	Micron N25Q512A11G1240F
FMC Connector (High-Pin):	Samtec ASP-134486-01
DDR3 SO-DIMM:	JAE MM80-204B1-1, MM80-204B1-E
MMCX Connector:	Samtec MMCX-J-P-H-ST-TH1
PMOD Connector:	Samtec SSW-106-01-F-D
USB3.0 Connector:	TE Connectivity 1932259-1
General-Purpose I/F(GPIO):	FCI 68001-110HLF

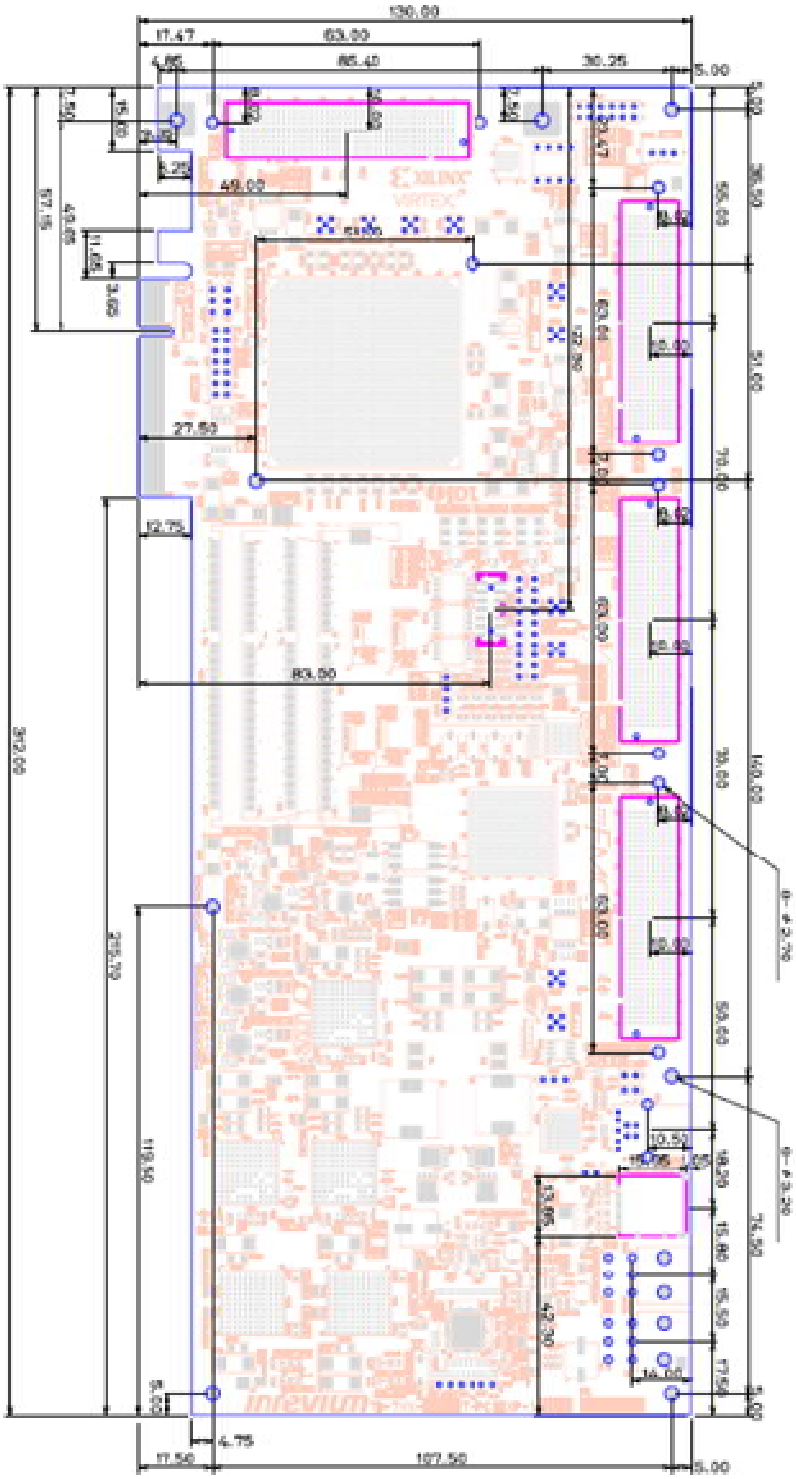

Figure 6-1 Board Dimension Diagram

7. Description of Each Component

7.1. Power Supply Structure

The following figure provides the internal power supply structure. The power is provided through a 12V ATX power connector.

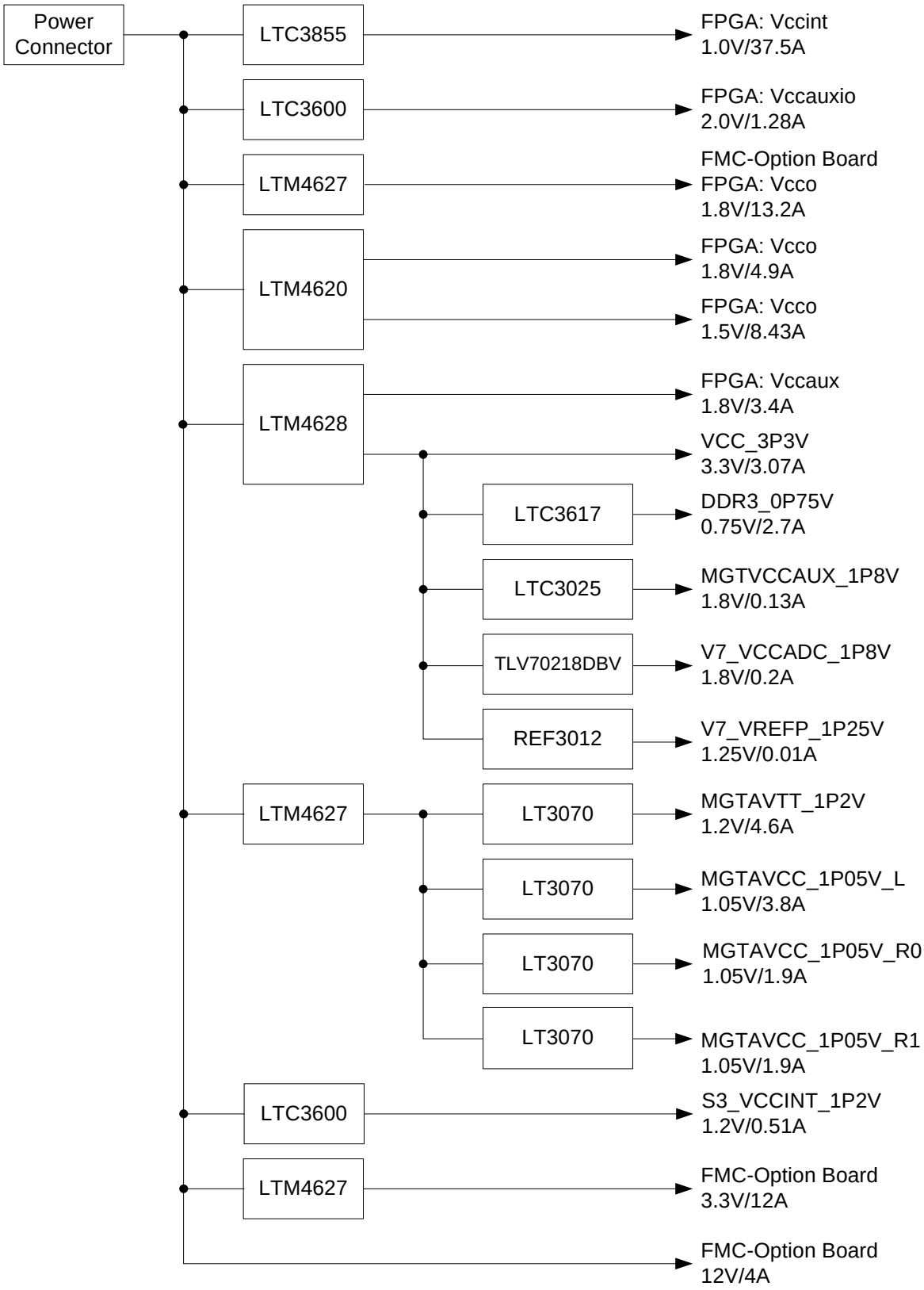

Figure 7-1 Power Supply Structure

7.2. Oscillator

This board provides the following clock sources.

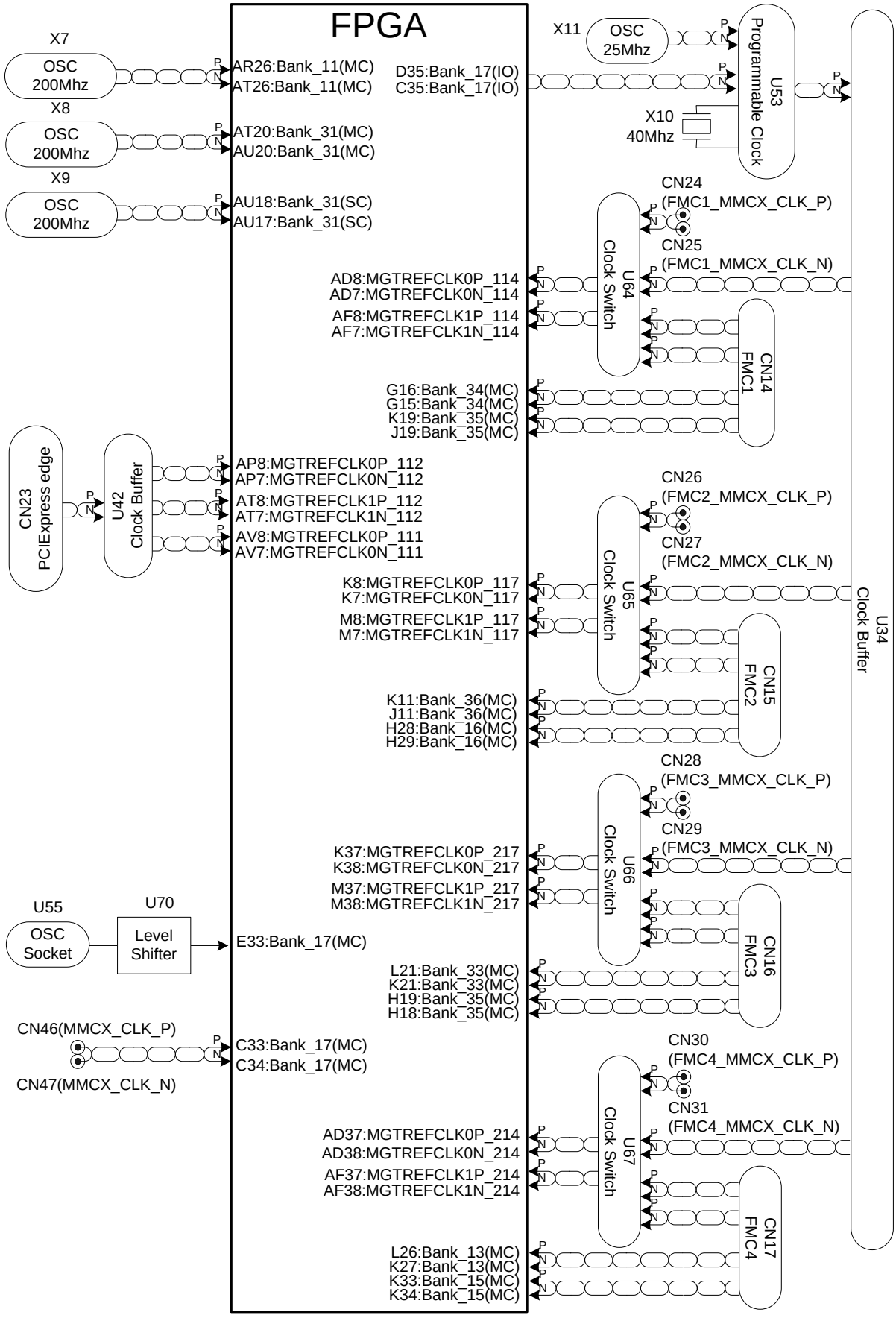

Figure 7-2 Clock Structure

Table 7-1 Details of Onboard Oscillator

Source	Signal Name	Signal Format	FPGA Pin#	Note
X7	DDR3_IF_1_CLK_200MHz_P /N	LVDS	AR26/AT26	DDR3_IF_1 system clock
X8	CLK_200M_P/N	LVDS	AT20/AU20	User clock
X9	DDR3_IF_2_CLK_200MHz_P/N	LVDS	AU18/AU17	DDR3_IF_2 system clock
CN23	PCIE_100M_REFCLK_P/N PCIE_125M_REFCLK_P/N PCIE_250M_REFCLK_P/N	LVDS	AP8/AP7 AT8/AT7 AV8/AV7	PIC Express Edge to differential buffer
U55	V7_RSVCLK	LVCMOS18	E33	OSC Socket spare clock
CN46 CN47	MMCX_CLK_P/N	LVDS	C33/C34	MMCX external supplied clock
U53	PLL_CLK_P/N	LVDS		Programmable clock(U53) generate device Source clock is OSC or FPGA.
U64	FMC1_MGTREFCLK0_P/N FMC1_MGTREFCLK1_P/N	LVDS	AD8/AD7 AF8/AF7	Programmable clock(U53) or MMCX (CN24/CN25), FMC1(CN14), MGT reference clock 0/1
CN14	FMC1_CLK0_M2C_P/N FMC1_CLK1_M2C_P/N	LVDS	G16/G15 K19/J19	FMC1 reference clock 0/1
U65	FMC2_MGTREFCLK0_P/N FMC2_MGTREFCLK1_P/N	LVDS	K8/K7 M8/M7	Programmable clock(U53) or MMCX (CN26/CN27), FMC2(CN15), MGT reference clock 0/1
CN15	FMC2_CLK0_M2C_P/N FMC2_CLK1_M2C_P/N	LVDS	K11/J11 H28/H29	FMC2 reference clock 0/1
U66	FMC3_MGTREFCLK0_P/N FMC3_MGTREFCLK1_P/N	LVDS	K37/K38 M37/M38	Programmable clock(U53) or MMCX (CN28/CN29) FMC3(CN16) MGT reference clock 0/1
CN16	FMC3_CLK0_M2C_P/N FMC3_CLK1_M2C_P/N	LVDS	L21/K21 H19/H18	FMC3 reference clock 0/1
U67	FMC4_MGTREFCLK0_P/N FMC4_MGTREFCLK1_P/N	LVDS	AD37/AD38 AF37/AF38	Programmable clock(U53) MMCX (CN30/CN31) FMC4(CN17) MGT reference clock 0/1
CN17	FMC4_CLK0_M2C_P/N FMC4_CLK1_M2C_P/N	LVDS	L26/K27 K33/K34	FMC4 reference clock 0/1

7.2.1. Programmable clock generator

This board has a programmable clock generater "ICS849N202I(U53)" for reference clock of Virtex-7 FPGA GTH Transceiver.

The initial setting is below.

- ICS849N202I: 156.25MHz
- SW5: all OFF.

Please used by default settings.

If using ICS849N202I for other frequency, please feel free to contact our support web

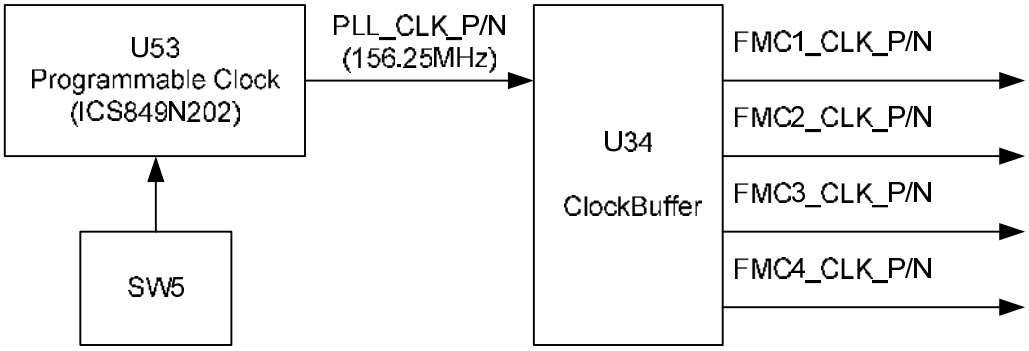

Figure 7-3 Programable Clock Connection

Output clock is distributed by Clock buffer(U34) then clocks are provide to each GTH group.

7.2.2. Clock Switch

Reference clock of GTH is selectable by "SN65LVDS250(U64,U65,U66,U67)"
Clock Switch has 4 clock sources and select 2 clocks for GTH reference clock.

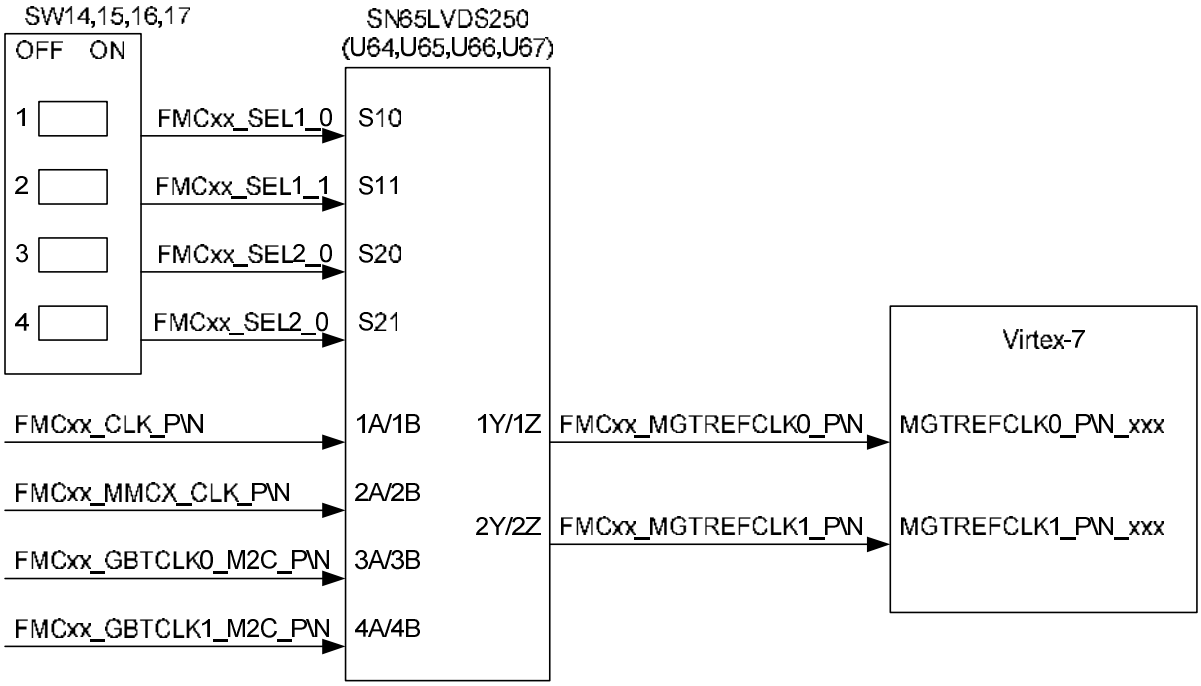

Figure 7-4 Connection of clock switch

Clock Sources

- FMCxx_CLK_P/N: From ICS849N202I programmable clock.
- FMCxx_MMCX_CLK_P/N: From MMCX(CN24,25/CN26,27/CN28,29/CN30.31).
- FMCxxx_GBTCLK0_M2C_P/N: From FMC(GBTCLK0_M2C_P/N)
- FMCxxx_GBTCLK1_M2C_P/N: From FMC(GBTCLK1_M2C_P/N)

Which Switch is related which FMC.

FMC1(CN14) : SW14
FMC2(CN15) : SW15
FMC3(CN16) : SW16
FMC4(CN17) : SW17

Table 7-2 Clock Selection

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2		
S10	S11	1Y/1Z	S20	S21	2Y/2Z
OFF	OFF	1A/1B	OFF	OFF	1A/1B
OFF	ON	2A/2B	OFF	ON	2A/2B
ON	OFF	3A/3B	ON	OFF	3A/3B
ON	ON	4A/4B	ON	ON	4A/4B

7.3. FMC Connector Interface

This board has 4 Samtec FMC connectors.

High-Pin Count: 4 (CN14,CN15,CN16,CN17)

The following provides the pinout table. Note that all pins are not connected to the FPGA.

Figure 7-5 High-Pin Count Pin Layout

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

7.3.1. FMC1 HPC Connector (High-Pin Count)

The board uses the High-Pin Count connector. Due to limitation of the number of FPGA pins (Banks), all FMC connector pins are not connected. The connector is interfaced as shown below.

HighSpead: TX 10ch, RX 10ch

LowSpead: LA 36Pair (include 2 pair clocks)

Table 7-3 FMC1 Connector Pinout

Bank No.	Pin No.	A		B	Pin No.	Bank No.
		GND	1	RES1		
MGTHRXP1_113	AL6	DP1_M2C_P	2	GND		
MGTHRXN1_113	AL5	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	Y4	MGTHRXP1_115
		GND	5	DP9_M2C_N	Y3	MGTHRXN1_115
MGTHRXP2_113	AJ6	DP2_M2C_P	6	GND		
MGTHRXN2_113	AJ5	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	AA6	MGTHRXP0_115
		GND	9	DP8_M2C_N	AA5	MGTHRXN0_115
MGTHRXP3_113	AH4	DP3_M2C_P	10	GND		
MGTHRXN3_113	AH3	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	AC6	MGTHRXP3_114
		GND	13	DP7_M2C_N	AC5	MGTHRXN3_114
MGTHRXP0_114	AG6	DP4_M2C_P	14	GND		
MGTHRXN0_114	AG5	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	AD4	MGTHRXP2_114
		GND	17	DP6_M2C_N	AD3	MGTHRXN2_114
MGTHRXP1_114	AE6	DP5_M2C_P	18	GND		
MGTHRXN1_114	AE5	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P		Clock Switch
		GND	21	*1 GBTCLK1_M2C_N		Clock Switch
MGTHTXP1_113	AL2	DP1_C2M_P	22	GND		
MGTHTXN1_113	AL1	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	AA2	MGTHTXP1_115
		GND	25	DP9_C2M_N	AA1	MGTHTXN1_115
MGTHTXP2_113	AK4	DP2_C2M_P	26	GND		
MGTHTXN2_113	AK3	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	AB4	MGTHTXP0_115
		GND	29	DP8_C2M_N	AB3	MGTHTXN0_115
MGTHTXP3_113	AJ2	DP3_C2M_P	30	GND		
MGTHTXN3_113	AJ1	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	AC2	MGTHTXP3_114
		GND	33	DP7_C2M_N	AC1	MGTHTXN3_114
MGTHTXP0_114	AG2	DP4_C2M_P	34	GND		
MGTHTXN0_114	AG1	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	AE2	MGTHTXP2_114
		GND	37	DP6_C2M_N	AE1	MGTHTXN2_114
MGTHTXP1_114	AF4	DP5_C2M_P	38	GND		
MGTHTXN1_114	AF3	DP5_C2M_N	39	GND		
		GND	40	RES0		

Bank No.	Pin No.	C		D	Pin No.	Bank No.
		GND	1	PG_C2M		
MGTHTXP0_113	AN2	DP0_C2M_P	2	GND		
MGTHTXN0_113	AN1	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P		Clock Switch
		GND	5	*1 GBTCLK0_M2C_N		Clock Switch
MGTHRXP0_113	AM4	DP0_M2C_P	6	GND		
MGTHRXN0_113	AM3	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	K16	34
		GND	9	LA01_N_CC	J16	34
34	J15	LA06_P	10	GND		
34	H15	LA06_N	11	LA05_P	K14	34
		GND	12	LA05_N	J14	34
		GND	13	GND		
34	G13	LA10_P	14	LA09_P	C12	34
34	F13	LA10_N	15	LA09_N	B12	34
		GND	16	GND		
		GND	17	LA13_P	U16	34
34	U15	LA14_P	18	LA13_N	T16	34
34	T15	LA14_N	19	GND		
		GND	20	LA17_P_CC	P14	34
		GND	21	LA17_N_CC	N14	34
34	T14	LA18_P_CC	22	GND		
34	R14	LA18_N_CC	23	LA23_P	K17	35
		GND	24	LA23_N	J17	35
		GND	25	GND		
35	L19	LA27_P	26	LA26_P	J20	35
35	K18	LA27_N	27	LA26_N	H20	35
		GND	28	GND		
		GND	29	TCK		
		SCL	30	*2 TDI		
		SDA	31	*2 TDO		
		GND	32	3P3VAUX		
		GND	33	TMS		
		GA0	34	TRST_L		
		12P0V	35	GA1		
		GND	36	3P3V		
		12P0V	37	GND		
		GND	38	3P3V		
		3P3V	39	GND		
		GND	40	3P3V		

Bank No.	Pin No.	E		F	Pin No.	Bank No.
		GND	1	PG_M2C		
		HA01_P_CC	2	GND		
		HA01_N_CC	3	GND		
		GND	4	HA00_P_CC		
		GND	5	HA00_N_CC		
		HA05_P	6	GND		
		HA05_N	7	HA04_P		
		GND	8	HA04_N		
		HA09_P	9	GND		
		HA09_N	10	HA08_P		
		GND	11	HA08_N		
		HA13_P	12	GND		
		HA13_N	13	HA12_P		
		GND	14	HA12_N		
		HA16_P	15	GND		
		HA16_N	16	HA15_P		
		GND	17	HA15_N		
		HA20_P	18	GND		
		HA20_N	19	HA19_P		
		GND	20	HA19_N		
		HB03_P	21	GND		
		HB03_N	22	HB02_P		
		GND	23	HB02_N		
		HB05_P	24	GND		
		HB05_N	25	HB04_P		
		GND	26	HB04_N		
		HB09_P	27	GND		
		HB09_N	28	HB08_P		
		GND	29	HB08_N		
		HB13_P	30	GND		
		HB13_N	31	HB12_P		
		GND	32	HB12_N		
		HB19_P	33	GND		
		HB19_N	34	HB16_P		
		GND	35	HB16_N		
		HB21_P	36	GND		
		HB21_N	37	HB20_P		
		GND	38	HB20_N		
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	VREF_A_M2C		
35	K19	CLK1_M2C_P	2	PRSNT_M2C_L		
35	J19	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	G16	34
		GND	5	CLK0_M2C_N	G15	34
34	B16	LA00_P_CC	6	GND		
34	A16	LA00_N_CC	7	LA02_P	C15	34
		GND	8	LA02_N	B15	34
34	A15	LA03_P	9	GND		
34	A14	LA03_N	10	LA04_P	B13	34
		GND	11	LA04_N	A13	34
34	C14	LA08_P	12	GND		
34	C13	LA08_N	13	LA07_P	D15	34
		GND	14	LA07_N	D14	34
34	E14	LA12_P	15	GND		
34	E13	LA12_N	16	LA11_P	F15	34
		GND	17	LA11_N	F14	34
34	F16	LA16_P	18	GND		
34	E16	LA16_N	19	LA15_P	H14	34
		GND	20	LA15_N	H13	34
34	M16	LA20_P	21	GND		
34	L16	LA20_N	22	LA19_P	L15	34
		GND	23	LA19_N	L14	34
34	N15	LA22_P	24	GND		
34	M15	LA22_N	25	LA21_P	P16	34
		GND	26	LA21_N	P15	34
35	M18	LA25_P	27	GND		
35	L18	LA25_N	28	LA24_P	N17	35
		GND	29	LA24_N	M17	35
35	N19	LA29_P	30	GND		
35	N18	LA29_N	31	LA28_P	R17	35
		GND	32	LA28_N	P17	35
35	T18	LA31_P	33	GND		
35	R18	LA31_N	34	LA30_P	T19	35
		GND	35	LA30_N	R19	35
35	U18	LA33_P	36	GND		
35	U17	LA33_N	37	LA32_P	V19	35
		GND	38	LA32_N	V18	35
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	J		K	Pin No.	Bank No.
		GND	1	VREF_B_M2C		
		CLK3_M2C_P	2	GND		
		CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P		
		GND	5	CLK2_M2C_N		
		HA03_P	6	GND		
		HA03_N	7	HA02_P		
		GND	8	HA02_N		
		HA07_P	9	GND		
		HA07_N	10	HA06_P		
		GND	11	HA06_N		
		HA11_P	12	GND		
		HA11_N	13	HA10_P		
		GND	14	HA10_N		
		HA14_P	15	GND		
		HA14_N	16	HA17_P_CC		
		GND	17	HA17_N_CC		
		HA18_P	18	GND		
		HA18_N	19	HA21_P		
		GND	20	HA21_N		
		HA22_P	21	GND		
		HA22_N	22	HA23_P		
		GND	23	HA23_N		
		HB01_P	24	GND		
		HB01_N	25	HB00_P_CC		
		GND	26	HB00_N_CC		
		HB07_P	27	GND		
		HB07_N	28	HB06_P_CC		
		GND	29	HB06_N_CC		
		HB11_P	30	GND		
		HB11_N	31	HB10_P		
		GND	32	HB10_N		
		HB15_P	33	GND		
		HB15_N	34	HB14_P		
		GND	35	HB14_N		
		HB18_P	36	GND		
		HB18_N	37	HB17_P_CC		
		GND	38	HB17_N_CC		
		*3 VIO_B_M2C	39	GND		
		GND	40	*3 VIO_B_M2C		

*1 GBTCLK0_M2C_P/N, GBTCLK1_M2C_P/N0

It will be MGT reference clock in case it is selected by U64 (clock selector) from FMC option card.

*2 FMC1 - JTAG (TDI, TDO)

TDI and TDO have a loopback structure for JTAG communication from the FMC mezzanine card.

*3 VIO_B_M2C

VIO_B_M2C is connected to FMC_VADJ power supply to increase power capacity.

*4 Power Supply

The board provides a 12V to the 12P0V pin and a 3.3V to the 3P3V and 3P3VAUX pins.
Also, 1.8V for VADJ pin.

7.3.2. FMC2 HPC Connector (High-Pin Count)

The board uses the High-Pin Count connector. Due to limitation of the number of FPGA pins (Banks), all FMC connector pins are not connected. The connector is interfaced as shown below.

HighSpead: TX 10ch, RX 10ch

LowSpead: LA 36Pair (include 2 pair clocks)

Table 7-4 FMC2 Connector Pinout

Bank No.	Pin No.	A		B	Pin No.	Bank No.
		GND	1	RES1		
MGTHRXP1_116	R6	DP1_M2C_P	2	GND		
MGTHRXN1_116	R5	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	D4	MGTHRXP1_118
		GND	5	DP9_M2C_N	D3	MGTHRXN1_118
MGTHRXP2_116	N6	DP2_M2C_P	6	GND		
MGTHRXN2_116	N5	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	E6	MGTHRXP0_118
		GND	9	DP8_M2C_N	E5	MGTHRXN0_118
MGTHRXP3_116	M4	DP3_M2C_P	10	GND		
MGTHRXN3_116	M3	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	G6	MGTHRXP3_117
		GND	13	DP7_M2C_N	G5	MGTHRXN3_117
MGTHRXP0_117	L6	DP4_M2C_P	14	GND		
MGTHRXN0_117	L5	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	H4	MGTHRXP2_117
		GND	17	DP6_M2C_N	H3	MGTHRXN2_117
MGTHRXP1_117	J6	DP5_M2C_P	18	GND		
MGTHRXN1_117	J5	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P		Clock Switch
		GND	21	*1 GBTCLK1_M2C_N		Clock Switch
MGTHTXP1_116	R2	DP1_C2M_P	22	GND		
MGTHTXN1_116	R1	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	E2	MGTHTXP1_118
		GND	25	DP9_C2M_N	E1	MGTHTXN1_118
MGTHTXP2_116	P4	DP2_C2M_P	26	GND		
MGTHTXN2_116	P3	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	F4	MGTHTXP0_118
		GND	29	DP8_C2M_N	F3	MGTHTXN0_118
MGTHTXP3_116	N2	DP3_C2M_P	30	GND		
MGTHTXN3_116	N1	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	G2	MGTHTXP3_117
		GND	33	DP7_C2M_N	G1	MGTHTXN3_117
MGTHTXP0_117	L2	DP4_C2M_P	34	GND		
MGTHTXN0_117	L1	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	J2	MGTHTXP2_117
		GND	37	DP6_C2M_N	J1	MGTHTXN2_117
MGTHTXP1_117	K4	DP5_C2M_P	38	GND		
MGTHTXN1_117	K3	DP5_C2M_N	39	GND		
		GND	40	RES0		

Bank No.	Pin No.	C		D	Pin No.	Bank No.
		GND	1	PG_C2M		
MGTHTXP0_116	U2	DP0_C2M_P	2	GND		
MGTHTXN0_116	U1	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P		Clock Switch
		GND	5	*1 GBTCLK0_M2C_N		Clock Switch
MGTHRXP0_116	T4	DP0_M2C_P	6	GND		
MGTHRXN0_116	T3	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	U13	36
		GND	9	LA01_N_CC	U12	36
36	T13	LA06_P	10	GND		
36	R13	LA06_N	11	LA05_P	N13	36
		GND	12	LA05_N	N12	36
		GND	13	GND		
36	M13	LA10_P	14	LA09_P	K13	36
36	L13	LA10_N	15	LA09_N	K12	36
		GND	16	GND		
		GND	17	LA13_P	J12	36
36	G12	LA14_P	18	LA13_N	H12	36
36	G11	LA14_N	19	GND		
		GND	20	LA17_P_CC	F11	36
		GND	21	LA17_N_CC	E11	36
36	E12	LA18_P_CC	22	GND		
36	D12	LA18_N_CC	23	LA23_P	C29	16
		GND	24	LA23_N	C30	16
		GND	25	GND		
16	B30	LA27_P	26	LA26_P	A28	16
16	A30	LA27_N	27	LA26_N	A29	16
		GND	28	GND		
		GND	29	TCK		
		SCL	30	*2 TDI		
		SDA	31	*2 TDO		
		GND	32	3P3VAUX		
		GND	33	TMS		
		GA0	34	TRST_L		
		12P0V	35	GA1		
		GND	36	3P3V		
		12P0V	37	GND		
		GND	38	3P3V		
		3P3V	39	GND		
		GND	40	3P3V		

Bank No.	PinNo.	E		F	Pin No.	Bank No.
		GND	1	PG_M2C		
		HA01_P_CC	2	GND		
		HA01_N_CC	3	GND		
		GND	4	HA00_P_CC		
		GND	5	HA00_N_CC		
		HA05_P	6	GND		
		HA05_N	7	HA04_P		
		GND	8	HA04_N		
		HA09_P	9	GND		
		HA09_N	10	HA08_P		
		GND	11	HA08_N		
		HA13_P	12	GND		
		HA13_N	13	HA12_P		
		GND	14	HA12_N		
		HA16_P	15	GND		
		HA16_N	16	HA15_P		
		GND	17	HA15_N		
		HA20_P	18	GND		
		HA20_N	19	HA19_P		
		GND	20	HA19_N		
		HB03_P	21	GND		
		HB03_N	22	HB02_P		
		GND	23	HB02_N		
		HB05_P	24	GND		
		HB05_N	25	HB04_P		
		GND	26	HB04_N		
		HB09_P	27	GND		
		HB09_N	28	HB08_P		
		GND	29	HB08_N		
		HB13_P	30	GND		
		HB13_N	31	HB12_P		
		GND	32	HB12_N		
		HB19_P	33	GND		
		HB19_N	34	HB16_P		
		GND	35	HB16_N		
		HB21_P	36	GND		
		HB21_N	37	HB20_P		
		GND	38	HB20_N		
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	VREF_A_M2C		
16	H28	CLK1_M2C_P	2	PRSNT_M2C_L		
16	H29	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	K11	36
		GND	5	CLK0_M2C_N	J11	36
36	U11	LA00_P_CC	6	GND		
36	U10	LA00_N_CC	7	LA02_P	T11	36
		GND	8	LA02_N	T10	36
36	R12	LA03_P	9	GND		
36	R11	LA03_N	10	LA04_P	P12	36
		GND	11	LA04_N	P11	36
36	N10	LA08_P	12	GND		
36	M10	LA08_N	13	LA07_P	M12	36
		GND	14	LA07_N	M11	36
36	L11	LA12_P	15	GND		
36	L10	LA12_N	16	LA11_P	J10	36
		GND	17	LA11_N	H10	36
36	G10	LA16_P	18	GND		
36	F10	LA16_N	19	LA15_P	D11	36
		GND	20	LA15_N	D10	36
36	A10	LA20_P	21	GND		
36	A9	LA20_N	22	LA19_P	B8	36
		GND	23	LA19_N	A8	36
36	B11	LA22_P	24	GND		
36	A11	LA22_N	25	LA21_P	C10	36
		GND	26	LA21_N	B10	36
16	B27	LA25_P	27	GND		
16	B28	LA25_N	28	LA24_P	C27	16
		GND	29	LA24_N	C28	16
16	D29	LA29_P	30	GND		
16	D30	LA29_N	31	LA28_P	E27	16
		GND	32	LA28_N	D27	16
16	F28	LA31_P	33	GND		
16	F29	LA31_N	34	LA30_P	G27	16
		GND	35	LA30_N	G28	16
16	G30	LA33_P	36	GND		
16	F30	LA33_N	37	LA32_P	E28	16
		GND	38	LA32_N	E29	16
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	J		K	PinNo.	Bank No.
		GND	1	VREF_B_M2C		
		CLK3_M2C_P	2	GND		
		CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P		
		GND	5	CLK2_M2C_N		
		HA03_P	6	GND		
		HA03_N	7	HA02_P		
		GND	8	HA02_N		
		HA07_P	9	GND		
		HA07_N	10	HA06_P		
		GND	11	HA06_N		
		HA11_P	12	GND		
		HA11_N	13	HA10_P		
		GND	14	HA10_N		
		HA14_P	15	GND		
		HA14_N	16	HA17_P_CC		
		GND	17	HA17_N_CC		
		HA18_P	18	GND		
		HA18_N	19	HA21_P		
		GND	20	HA21_N		
		HA22_P	21	GND		
		HA22_N	22	HA23_P		
		GND	23	HA23_N		
		HB01_P	24	GND		
		HB01_N	25	HB00_P_CC		
		GND	26	HB00_N_CC		
		HB07_P	27	GND		
		HB07_N	28	HB06_P_CC		
		GND	29	HB06_N_CC		
		HB11_P	30	GND		
		HB11_N	31	HB10_P		
		GND	32	HB10_N		
		HB15_P	33	GND		
		HB15_N	34	HB14_P		
		GND	35	HB14_N		
		HB18_P	36	GND		
		HB18_N	37	HB17_P_CC		
		GND	38	HB17_N_CC		
		*3 VIO_B_M2C	39	GND		
		GND	40	*3 VIO_B_M2C		

*1 GBTCLK0_M2C_P/N, GBTCLK1_M2C_P/N0

It will be MGT reference clock in case it is selected by U65 (clock selector) from FMC option card.

*2 FMC1 -JTAG (TDI, TDO)

TDI and TDO have a loopback structure for JTAG communication from the FMC mezzanine card.

*3 VIO_B_M2C

VIO_B_M2C is connected to FMC_VADJ power supply to increase power capacity.

*4 Power Supply

The board provides a 12V to the 12P0V pin and a 3.3V to the 3P3V and 3P3VAUX pins.
Also, 1.8V for VADJ pin.

7.3.3. FMC3 HPC Connector (High-Pin Count)

The board uses the High-Pin Count connector. Due to limitation of the number of FPGA pins (Banks), all FMC connector pins are not connected. The connector is interfaced as shown below.

HighSpead: TX 10ch, RX 10ch

LowSpead: LA 36Pair (include 2 pair clocks)

Table 7-5 FMC3 Connector Pinout

Bank No.	Pin No.	A		B	Pin No.	Bank No.
		GND	1	RES1		
MGTHRXP1_216	R39	DP1_M2C_P	2	GND		
MGTHRXN1_216	R40	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	D41	MGTHRXP1_218
		GND	5	DP9_M2C_N	D42	MGTHRXN1_218
MGTHRXP2_216	N39	DP2_M2C_P	6	GND		
MGTHRXN2_216	N40	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	E39	MGTHRXP0_218
		GND	9	DP8_M2C_N	E40	MGTHRXN0_218
MGTHRXP3_216	M41	DP3_M2C_P	10	GND		
MGTHRXN3_216	M42	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	G39	MGTHRXP3_217
		GND	13	DP7_M2C_N	G40	MGTHRXN3_217
MGTHRXP0_217	L39	DP4_M2C_P	14	GND		
MGTHRXN0_217	L40	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	H41	MGTHRXP2_217
		GND	17	DP6_M2C_N	H42	MGTHRXN2_217
MGTHRXP1_217	J39	DP5_M2C_P	18	GND		
MGTHRXN1_217	J40	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P		Clock Switch
		GND	21	*1 GBTCLK1_M2C_N		Clock Switch
MGTHTXP1_216	R43	DP1_C2M_P	22	GND		
MGTHTXN1_216	R44	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	E43	MGTHTXP1_218
		GND	25	DP9_C2M_N	E44	MGTHTXN1_218
MGTHTXP2_216	P41	DP2_C2M_P	26	GND		
MGTHTXN2_216	P42	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	F41	MGTHTXP0_218
		GND	29	DP8_C2M_N	F42	MGTHTXN0_218
MGTHTXP3_216	N43	DP3_C2M_P	30	GND		
MGTHTXN3_216	N44	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	G43	MGTHTXP3_217
		GND	33	DP7_C2M_N	G44	MGTHTXN3_217
MGTHTXP0_217	L43	DP4_C2M_P	34	GND		
MGTHTXN0_217	L44	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	J43	MGTHTXP2_217
		GND	37	DP6_C2M_N	J44	MGTHTXN2_217
MGTHTXP1_217	K41	DP5_C2M_P	38	GND		
MGTHTXN1_217	K42	DP5_C2M_N	39	GND		
		GND	40	RES0		

Bank No.	Pin No.	C		D	Pin No.	Bank No.
		GND	1	PG_C2M		
MGTHTXP0_216	U43	DP0_C2M_P	2	GND		
MGTHTXN0_216	U44	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P		Clock Switch
		GND	5	*1 GBTCLK0_M2C_N		Clock Switch
MGTHRXP0_216	T41	DP0_M2C_P	6	GND		
MGTHRXN0_216	T42	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	D22	33
		GND	9	LA01_N_CC	D21	33
33	E22	LA06_P	10	GND		
33	E21	LA06_N	11	LA05_P	C23	33
		GND	12	LA05_N	B23	33
		GND	13	GND		
33	U21	LA10_P	14	LA09_P	R21	33
33	T21	LA10_N	15	LA09_N	P21	33
		GND	16	GND		
		GND	17	LA13_P	F23	33
33	M23	LA14_P	18	LA13_N	E23	33
33	L23	LA14_N	19	GND		
		GND	20	LA17_P_CC	K23	33
		GND	21	LA17_N_CC	K22	33
33	M22	LA18_P_CC	22	GND		
33	M21	LA18_N_CC	23	LA23_P	H17	35
		GND	24	LA23_N	G17	35
		GND	25	GND		
35	C18	LA27_P	26	LA26_P	A19	35
35	C17	LA27_N	27	LA26_N	A18	35
		GND	28	GND		
		GND	29	TCK		
		SCL	30	*2 TDI		
		SDA	31	*2 TDO		
		GND	32	3P3VAUX		
		GND	33	TMS		
		GA0	34	TRST_L		
		12P0V	35	GA1		
		GND	36	3P3V		
		12P0V	37	GND		
		GND	38	3P3V		
		3P3V	39	GND		
		GND	40	3P3V		

Bank No.	Pin No.	E		F	Pin No.	Bank No.
		GND	1	PG_M2C		
		HA01_P_CC	2	GND		
		HA01_N_CC	3	GND		
		GND	4	HA00_P_CC		
		GND	5	HA00_N_CC		
		HA05_P	6	GND		
		HA05_N	7	HA04_P		
		GND	8	HA04_N		
		HA09_P	9	GND		
		HA09_N	10	HA08_P		
		GND	11	HA08_N		
		HA13_P	12	GND		
		HA13_N	13	HA12_P		
		GND	14	HA12_N		
		HA16_P	15	GND		
		HA16_N	16	HA15_P		
		GND	17	HA15_N		
		HA20_P	18	GND		
		HA20_N	19	HA19_P		
		GND	20	HA19_N		
		HB03_P	21	GND		
		HB03_N	22	HB02_P		
		GND	23	HB02_N		
		HB05_P	24	GND		
		HB05_N	25	HB04_P		
		GND	26	HB04_N		
		HB09_P	27	GND		
		HB09_N	28	HB08_P		
		GND	29	HB08_N		
		HB13_P	30	GND		
		HB13_N	31	HB12_P		
		GND	32	HB12_N		
		HB19_P	33	GND		
		HB19_N	34	HB16_P		
		GND	35	HB16_N		
		HB21_P	36	GND		
		HB21_N	37	HB20_P		
		GND	38	HB20_N		
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	VREF_A_M2C		
35	H19	CLK1_M2C_P	2	PRSNT_M2C_L		
35	H18	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	L21	33
		GND	5	CLK0_M2C_N	K21	33
33	B21	LA00_P_CC	6	GND		
33	B20	LA00_N_CC	7	LA02_P	A21	33
		GND	8	LA02_N	A20	33
33	C22	LA03_P	9	GND		
33	B22	LA03_N	10	LA04_P	G21	33
		GND	11	LA04_N	F21	33
33	H22	LA08_P	12	GND		
33	G22	LA08_N	13	LA07_P	J22	33
		GND	14	LA07_N	J21	33
33	H23	LA12_P	15	GND		
33	G23	LA12_N	16	LA11_P	M20	33
		GND	17	LA11_N	L20	33
33	V22	LA16_P	18	GND		
33	U22	LA16_N	19	LA15_P	U23	33
		GND	20	LA15_N	T23	33
33	U20	LA20_P	21	GND		
33	T20	LA20_N	22	LA19_P	R22	33
		GND	23	LA19_N	P22	33
33	P20	LA22_P	24	GND		
33	N20	LA22_N	25	LA21_P	N23	33
		GND	26	LA21_N	N22	33
35	D17	LA25_P	27	GND		
35	D16	LA25_N	28	LA24_P	B18	35
		GND	29	LA24_N	B17	35
35	G18	LA29_P	30	GND		
35	F18	LA29_N	31	LA28_P	G20	35
		GND	32	LA28_N	F20	35
35	F19	LA31_P	33	GND		
35	E19	LA31_N	34	LA30_P	E18	35
		GND	35	LA30_N	E17	35
35	D20	LA33_P	36	GND		
35	D19	LA33_N	37	LA32_P	C20	35
		GND	38	LA32_N	C19	35
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	J		K	Pin No.	Bank No.
		GND	1	VREF_B_M2C		
		CLK3_M2C_P	2	GND		
		CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P		
		GND	5	CLK2_M2C_N		
		HA03_P	6	GND		
		HA03_N	7	HA02_P		
		GND	8	HA02_N		
		HA07_P	9	GND		
		HA07_N	10	HA06_P		
		GND	11	HA06_N		
		HA11_P	12	GND		
		HA11_N	13	HA10_P		
		GND	14	HA10_N		
		HA14_P	15	GND		
		HA14_N	16	HA17_P_CC		
		GND	17	HA17_N_CC		
		HA18_P	18	GND		
		HA18_N	19	HA21_P		
		GND	20	HA21_N		
		HA22_P	21	GND		
		HA22_N	22	HA23_P		
		GND	23	HA23_N		
		HB01_P	24	GND		
		HB01_N	25	HB00_P_CC		
		GND	26	HB00_N_CC		
		HB07_P	27	GND		
		HB07_N	28	HB06_P_CC		
		GND	29	HB06_N_CC		
		HB11_P	30	GND		
		HB11_N	31	HB10_P		
		GND	32	HB10_N		
		HB15_P	33	GND		
		HB15_N	34	HB14_P		
		GND	35	HB14_N		
		HB18_P	36	GND		
		HB18_N	37	HB17_P_CC		
		GND	38	HB17_N_CC		
		*3 VIO_B_M2C	39	GND		
		GND	40	*3 VIO_B_M2C		

*1 GBTCLK0_M2C_P/N, GBTCLK1_M2C_P/N0

It will be MGT reference clock in case it is selected by U66 (clock selector) from FMC option card.

*2 FMC1 - JTAG (TDI, TDO)

TDI and TDO have a loopback structure for JTAG communication from the FMC mezzanine card.

*3 VIO_B_M2C

VIO_B_M2C is connected to FMC_VADJ power supply to increase power capacity.

*4 Power Supply

The board provides a 12V to the 12P0V pin and a 3.3V to the 3P3V and 3P3VAUX pins.
Also, 1.8V for VADJ pin.

7.3.4. FMC4 HPC Connector (High-Pin Count)

The board uses the High-Pin Count connector. Due to limitation of the number of FPGA pins (Banks), all FMC connector pins are not connected. The connector is interfaced as shown below.

HighSpead: TX 10ch, RX 10ch

LowSpead: LA 36Pair (include 2 pair clocks)

Table 7-6 FMC4 Connector Pinout

Bank No.	Pin No.	A		B	Pin No.	Bank No.
		GND	1	RES1		
MGTHRXP1_213	AL39	DP1_M2C_P	2	GND		
MGTHRXN1_213	AL40	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	Y41	MGTHRXP1_215
		GND	5	DP9_M2C_N	Y42	MGTHRXN1_215
MGTHRXP2_213	AJ39	DP2_M2C_P	6	GND		
MGTHRXN2_213	AJ40	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	AA39	MGTHRXP0_215
		GND	9	DP8_M2C_N	AA40	MGTHRXN0_215
MGTHRXP3_213	AH41	DP3_M2C_P	10	GND		
MGTHRXN3_213	AH42	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	AC39	MGTHRXP3_214
		GND	13	DP7_M2C_N	AC40	MGTHRXN3_214
MGTHRXP0_214	AG39	DP4_M2C_P	14	GND		
MGTHRXN0_214	AG40	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	AD41	MGTHRXP2_214
		GND	17	DP6_M2C_N	AD42	MGTHRXN2_214
MGTHRXP1_214	AE39	DP5_M2C_P	18	GND		
MGTHRXN1_214	AE40	DP5_M2C_N	19	GND		
		GND	20	*1 GBTCLK1_M2C_P		Clock Switch
		GND	21	*1 GBTCLK1_M2C_N		Clock Switch
MGTHTXP1_213	AL43	DP1_C2M_P	22	GND		
MGTHTXN1_213	AL44	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	AA43	MGTHTXP1_215
		GND	25	DP9_C2M_N	AA44	MGTHTXN1_215
MGTHTXP2_213	AK41	DP2_C2M_P	26	GND		
MGTHTXN2_213	AK42	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	AB41	MGTHTXP0_215
		GND	29	DP8_C2M_N	AB42	MGTHTXN0_215
MGTHTXP3_213	AJ43	DP3_C2M_P	30	GND		
MGTHTXN3_213	AJ44	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	AC43	MGTHTXP3_214
		GND	33	DP7_C2M_N	AC44	MGTHTXN3_214
MGTHTXP0_214	AG43	DP4_C2M_P	34	GND		
MGTHTXN0_214	AG44	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	AE43	MGTHTXP2_214
		GND	37	DP6_C2M_N	AE44	MGTHTXN2_214
MGTHTXP1_214	AF41	DP5_C2M_P	38	GND		
MGTHTXN1_214	AF42	DP5_C2M_N	39	GND		
		GND	40	RES0		

Bank No.	Pin No.	C		D	Pin No.	Bank No.
		GND	1	PG_C2M		
MGTHTXP0_213	AN43	DP0_C2M_P	2	GND		
MGTHTXN0_213	AN44	DP0_C2M_N	3	GND		
		GND	4	*1 GBTCLK0_M2C_P		Clock Switch
		GND	5	*1 GBTCLK0_M2C_N		Clock Switch
MGTHRXP0_213	AM41	DP0_M2C_P	6	GND		
MGTHRXN0_213	AM42	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	T24	13
		GND	9	LA01_N_CC	R24	13
13	P24	LA06_P	10	GND		
13	P25	LA06_N	11	LA05_P	M26	13
		GND	12	LA05_N	M27	13
		GND	13	GND		
13	M25	LA10_P	14	LA09_P	L24	13
13	L25	LA10_N	15	LA09_N	K24	13
		GND	16	GND		
		GND	17	LA13_P	J24	13
13	H24	LA14_P	18	LA13_N	J25	13
13	H25	LA14_N	19	GND		
		GND	20	LA17_P_CC	A23	13
		GND	21	LA17_N_CC	A24	13
13	D24	LA18_P_CC	22	GND		
13	D25	LA18_N_CC	23	LA23_P	K31	15
		GND	24	LA23_N	J31	15
		GND	25	GND		
15	L31	LA27_P	26	LA26_P	J32	15
15	K32	LA27_N	27	LA26_N	H32	15
		GND	28	GND		
		GND	29	TCK		
		SCL	30	*2 TDI		
		SDA	31	*2 TDO		
		GND	32	3P3VAUX		
		GND	33	TMS		
		GA0	34	TRST_L		
		12P0V	35	GA1		
		GND	36	3P3V		
		12P0V	37	GND		
		GND	38	3P3V		
		3P3V	39	GND		
		GND	40	3P3V		

Bank No.	Pin No.	E		F	Pin No.	Bank No.
		GND	1	PG_M2C		
		HA01_P_CC	2	GND		
		HA01_N_CC	3	GND		
		GND	4	HA00_P_CC		
		GND	5	HA00_N_CC		
		HA05_P	6	GND		
		HA05_N	7	HA04_P		
		GND	8	HA04_N		
		HA09_P	9	GND		
		HA09_N	10	HA08_P		
		GND	11	HA08_N		
		HA13_P	12	GND		
		HA13_N	13	HA12_P		
		GND	14	HA12_N		
		HA16_P	15	GND		
		HA16_N	16	HA15_P		
		GND	17	HA15_N		
		HA20_P	18	GND		
		HA20_N	19	HA19_P		
		GND	20	HA19_N		
		HB03_P	21	GND		
		HB03_N	22	HB02_P		
		GND	23	HB02_N		
		HB05_P	24	GND		
		HB05_N	25	HB04_P		
		GND	26	HB04_N		
		HB09_P	27	GND		
		HB09_N	28	HB08_P		
		GND	29	HB08_N		
		HB13_P	30	GND		
		HB13_N	31	HB12_P		
		GND	32	HB12_N		
		HB19_P	33	GND		
		HB19_N	34	HB16_P		
		GND	35	HB16_N		
		HB21_P	36	GND		
		HB21_N	37	HB20_P		
		GND	38	HB20_N		
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	VREF_A_M2C		
15	K33	CLK1_M2C_P	2	PRSNT_M2C_L		
15	K34	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	L26	13
		GND	5	CLK0_M2C_N	K27	13
13	U26	LA00_P_CC	6	GND		
13	U27	LA00_N_CC	7	LA02_P	T25	13
		GND	8	LA02_N	T26	13
13	K26	LA03_P	9	GND		
13	J26	LA03_N	10	LA04_P	J27	13
		GND	11	LA04_N	H27	13
13	G25	LA08_P	12	GND		
13	G26	LA08_N	13	LA07_P	F25	13
		GND	14	LA07_N	F26	13
13	F24	LA12_P	15	GND		
13	E24	LA12_N	16	LA11_P	E26	13
		GND	17	LA11_N	D26	13
13	C24	LA16_P	18	GND		
13	C25	LA16_N	19	LA15_P	B25	13
		GND	20	LA15_N	B26	13
13	A25	LA20_P	21	GND		
13	A26	LA20_N	22	LA19_P	N24	13
		GND	23	LA19_N	N25	13
13	P26	LA22_P	24	GND		
13	P27	LA22_N	25	LA21_P	R26	13
		GND	26	LA21_N	R27	13
15	J34	LA25_P	27	GND		
15	J35	LA25_N	28	LA24_P	H33	15
		GND	29	LA24_N	H34	15
15	G32	LA29_P	30	GND		
15	G33	LA29_N	31	LA28_P	G31	15
		GND	32	LA28_N	F31	15
15	E31	LA31_P	33	GND		
15	D31	LA31_N	34	LA30_P	E32	15
		GND	35	LA30_N	D32	15
15	C32	LA33_P	36	GND		
15	B32	LA33_N	37	LA32_P	B31	15
		GND	38	LA32_N	A31	15
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	J		K	Pin No.	Bank No.
		GND	1	VREF_B_M2C		
		CLK3_M2C_P	2	GND		
		CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P		
		GND	5	CLK2_M2C_N		
		HA03_P	6	GND		
		HA03_N	7	HA02_P		
		GND	8	HA02_N		
		HA07_P	9	GND		
		HA07_N	10	HA06_P		
		GND	11	HA06_N		
		HA11_P	12	GND		
		HA11_N	13	HA10_P		
		GND	14	HA10_N		
		HA14_P	15	GND		
		HA14_N	16	HA17_P_CC		
		GND	17	HA17_N_CC		
		HA18_P	18	GND		
		HA18_N	19	HA21_P		
		GND	20	HA21_N		
		HA22_P	21	GND		
		HA22_N	22	HA23_P		
		GND	23	HA23_N		
		HB01_P	24	GND		
		HB01_N	25	HB00_P_CC		
		GND	26	HB00_N_CC		
		HB07_P	27	GND		
		HB07_N	28	HB06_P_CC		
		GND	29	HB06_N_CC		
		HB11_P	30	GND		
		HB11_N	31	HB10_P		
		GND	32	HB10_N		
		HB15_P	33	GND		
		HB15_N	34	HB14_P		
		GND	35	HB14_N		
		HB18_P	36	GND		
		HB18_N	37	HB17_P_CC		
		GND	38	HB17_N_CC		
		*3 VIO_B_M2C	39	GND		
		GND	40	*3 VIO_B_M2C		

*1 GBTCLK0_M2C_P/N, GBTCLK1_M2C_P/N0

It will be MGT reference clock in case it is selected by U67 (clock selector) from FMC option card.

*2 FMC1 -JTAG (TDI,TDO)

TDI and TDO have a loopback structure for JTAG communication from the FMC mezzanine card.

*3 VIO_B_M2C

VIO_B_M2C is connected to FMC_VADJ power supply to increase power capacity.

*4 Power Supply

The board provides a 12V to the 12P0V pin and a 3.3V to the 3P3V and 3P3VAUX pins.
Also, 1.8V for VADJ pin.

Notice:

On the FPGA GTH design for FMC4, please use a QPLL. If using a CPLL, GTH interface could be unstable. Please feel free to contact us for more details.

7.4. DDR3 SO-DIMM Interface

The board provides 2 Micron DDR3 SO-DIMM(4GByte).
On the PCB, bottom side is DIMM1 and top side is DIMM2.

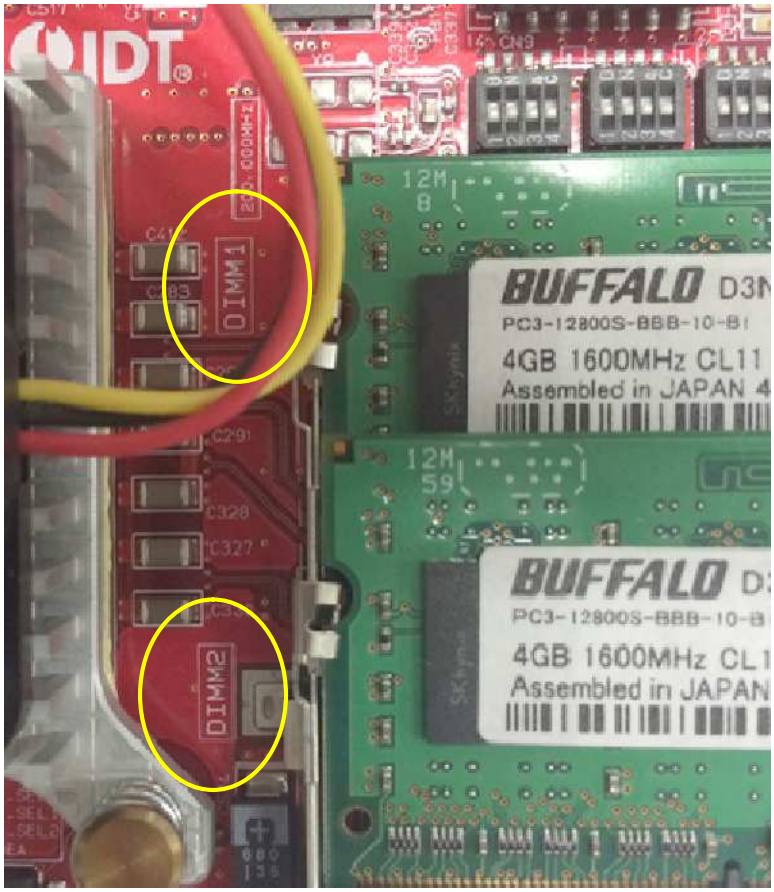

Figure 7-6 DIMM1 and DIMM2

Table 7-7 DDR3 SO-DIMM-1 Pinout

Bank No.	Pin No.	Signal Name	Pin No.		Signal Name	Pin No.	Bank No.
	-	VREFDQ	1	2	Vss	-	
	-	Vss	3	4	DQ4	AK22	12
12	AJ24	DQ0	5	6	DQ5	AL23	12
12	AK21	DQ1	7	8	Vss	-	
	-	Vss	9	10	DQS0#	AK23	12
12	AJ25	DM0	11	12	DQS0	AK24	12
	-	Vss	13	14	Vss	-	
12	AL21	DQ2	15	16	DQ6	AM23	12
12	AJ22	DQ3	17	18	DQ7	AM22	12
	-	Vss	19	20	Vss	-	
12	AP24	DQ8	21	22	DQ12	AN22	12
12	AP22	DQ9	23	24	DQ13	AT24	12
	-	Vss	25	26	Vss	-	
12	AR23	DQS1#	27	28	DM1	AN24	12
12	AR24	DQS1	29	30	RESET#	AR21	12
	-	Vss	31	32	Vss	-	
12	AP21	DQ10	33	34	DQ14	AT23	12
12	AN23	DQ11	35	36	DQ15	AR22	12
	-	Vss	37	38	Vss	-	
12	AT21	DQ16	39	40	DQ20	AV22	12
12	AU21	DQ17	41	42	DQ21	AY22	12
	-	Vss	43	44	Vss	-	
12	AW21	DQS2#	45	46	DM2	AV23	12
12	AW22	DQS2	47	48	Vss	-	
	-	Vss	49	50	DQ22	AY21	12
12	AU23	DQ18	51	52	DQ23	AV24	12
12	AU22	DQ19	53	54	Vss	-	
	-	Vss	55	56	DQ28	BB23	12
12	BA21	DQ24	57	58	DQ29	BB22	12
12	BB21	DQ25	59	60	Vss	-	
	-	Vss	61	62	DQS3#	BA23	12
12	AY24	DM3	63	64	DQS3	BA24	12
	-	Vss	65	66	Vss	-	
12	BC22	DQ26	67	68	DQ30	BC24	12
12	BD22	DQ27	69	70	DQ31	BC23	12
	-	Vss	71	72	Vss	-	
11	AW27	CKE0	73	74	CKE1	AY27	11

Bank No.	Pin No.	Signal Name	Pin No.		Signal Name	Pin No.	Bank No.
	-	VDD	75	76	VDD	-	
	-	NC	77	78	A15	AH27	11
11	AN25	BA2	79	80	A14	AH28	11
	-	VDD	81	82	VDD	-	
11	AJ27	A12	83	84	A11	AK27	11
11	AK29	A9	85	86	A7	AK26	11
	-	VDD	87	88	VDD	-	
11	AL29	A8	89	90	A6	AL26	11
11	AM27	A5	91	92	A4	AM28	11
	-	VDD	93	94	VDD	-	
11	AM25	A3	95	96	A2	AM26	11
11	AN27	A1	97	98	A0	AN28	11
	-	VDD	99	100	VDD	-	
11	AH29	CK0	101	102	CK1	AU27	11
11	AJ29	CK0#	103	104	CK1#	AV27	11
	-	VDD	105	106	VDD	-	
11	AK28	A10	107	108	BA1	AP25	11
11	AR27	BA0	109	110	RAS#	AR28	11
	-	VDD	111	112	VDD	-	
11	AP27	WE#	113	114	CS0#	AU25	11
11	AP26	CAS#	115	116	ODT0	AW25	11
	-	VDD	117	118	VDD	-	
11	AJ26	A13	119	120	ODT1	AW26	11
11	AV25	CS1	121	122	NC	-	
	-	VDD	123	124	VDD	-	
	-	NC	125	126	VREFCA	-	
	-	Vss	127	128	Vss	-	
10	AL31	DQ32	129	130	DQ36	AM31	10
10	AJ30	DQ33	131	132	DQ37	AM32	10
	-	Vss	133	134	Vss	-	
10	AN30	DQS4#	135	136	DM4	AK31	10
10	AM30	DQS4	137	138	Vss	-	
	-	Vss	139	140	DQ38	AN32	10
10	AJ31	DQ34	141	142	DQ39	AN29	10
10	AL30	DQ35	143	144	Vss	-	
	-	Vss	145	146	DQ44	AY32	10
10	BA28	DQ40	147	148	DQ45	AV29	10
10	BA30	DQ41	149	150	Vss	-	
	-	Vss	151	152	DQS5#	BA29	10
10	AY28	DM5	153	154	DQS5	AY29	10
	-	Vss	155	156	Vss	-	
10	BA31	DQ42	157	158	DQ46	AW29	10
10	AY31	DQ43	159	160	DQ47	AW30	10
	-	Vss	161	162	Vss	-	

Bank No.	Pin No.	Signal Name	Pin No.		Signal Name	Pin No.	Bank No.
10	AU30	DQ48	163	164	DQ52	AT30	10
10	AV30	DQ49	165	166	DQ53	AT31	10
	-	Vss	167	168	Vss	-	
10	AR31	DQS6#	169	170	DM6	AR29	10
10	AP31	DQS6	171	172	Vss	-	
	-	Vss	173	174	DQ54	AU31	10
10	AU28	DQ50	175	176	DQ55	AT28	10
10	AV28	DQ51	177	178	Vss	-	
	-	Vss	179	180	DQ60	BB32	10
10	BB28	DQ56	181	182	DQ61	BC32	10
10	BC28	DQ57	183	184	Vss	-	
	-	Vss	185	186	DQS7#	BD32	10
10	BB30	DM7	187	188	DQS7	BD31	10
	-	Vss	189	190	Vss	-	
10	BC29	DQ58	191	192	DQ62	BC30	10
10	BD29	DQ59	193	194	DQ63	BD30	10
	-	Vss	195	196	Vss	-	
	-	SA0	197	198	EVENT#	-	
	-	VDDSPD	199	200	SDA		
	-	SA1	201	202	SCL		
	-	VTT	203	204	VTT	-	

Table 7-8 DDR3 SO-DIMM-2 Pinout Table

Bank No.	Pin No.	Signal Name	Pin No.		Signal Name	Pin No.	Bank No.
	-	VREFDQ	1	2	Vss	-	
	-	Vss	3	4	DQ4	AJ10	32
32	AL11	DQ0	5	6	DQ5	AM12	32
32	AH12	DQ1	7	8	Vss	-	
	-	Vss	9	10	DQS0#	AM10	32
32	AK11	DM0	11	12	DQS0	AL10	32
	-	Vss	13	14	Vss	-	
32	AJ12	DQ2	15	16	DQ6	AM11	32
32	AJ11	DQ3	17	18	DQ7	AK13	32
	-	Vss	19	20	Vss	-	
32	AP10	DQ8	21	22	DQ12	AP12	32
32	AM13	DQ9	23	24	DQ13	AT11	32
	-	Vss	25	26	Vss	-	
32	AR11	DQS1#	27	28	DM1	AN10	32
32	AP11	DQS1	29	30	RESET#	AR12	32
	-	Vss	31	32	Vss	-	
32	AN13	DQ10	33	34	DQ14	AT10	32
32	AN12	DQ11	35	36	DQ15	AR13	32
	-	Vss	37	38	Vss	-	
32	AU11	DQ16	39	40	DQ20	AY11	32
32	AU10	DQ17	41	42	DQ21	BA11	32
	-	Vss	43	44	Vss	-	
32	AW10	DQS2#	45	46	DM2	AW11	32
32	AV10	DQS2	47	48	Vss	-	
	-	Vss	49	50	DQ22	BA10	32
32	AU12	DQ18	51	52	DQ23	AW12	32
32	AV12	DQ19	53	54	Vss	-	
	-	Vss	55	56	DQ28	BC10	32
32	BD10	DQ24	57	58	DQ29	BC9	32
32	BD9	DQ25	59	60	Vss	-	
	-	Vss	61	62	DQS3#	BC8	32
32	BB11	DM3	63	64	DQS3	BB8	32
	-	Vss	65	66	Vss	-	
32	BB12	DQ26	67	68	DQ30	BD12	32
32	BC12	DQ27	69	70	DQ31	BD11	32
	-	Vss	71	72	Vss	-	
31	AV20	CKE0	73	74	CKE1	AW20	31

Bank No.	Pin No.	Signal Name	Pin No.		Signal Name	Pin No.	Bank No.
	-	VDD	75	76	VDD	-	
	-	NC	77	78	A15	AK18	31
31	AM17	BA2	79	80	A14	AK17	31
	-	VDD	81	82	VDD	-	
31	AH17	A12	83	84	A11	AJ20	31
31	AL20	A9	85	86	A7	AK19	31
	-	VDD	87	88	VDD	-	
31	AM20	A8	89	90	A6	AL19	31
31	AN19	A5	91	92	A4	AN18	31
	-	VDD	93	94	VDD	-	
31	AP17	A3	95	96	A2	AR17	31
31	AP20	A1	97	98	A0	AP19	31
	-	VDD	99	100	VDD	-	
31	AL18	CK0	101	102	CK1	AW19	31
31	AM18	CK0#	103	104	CK1#	AY19	31
	-	VDD	105	106	VDD	-	
31	AJ19	A10	107	108	BA1	AN17	31
31	AR19	BA0	109	110	RAS#	AR18	31
	-	VDD	111	112	VDD	-	
31	AT18	WE#	113	114	CS0#	AV19	31
31	AT19	CAS#	115	116	ODT0	AV17	31
	-	VDD	117	118	VDD	-	
31	AH18	A13	119	120	ODT1	AW17	31
31	AV18	CS1	121	122	NC	-	
	-	VDD	123	124	VDD	-	
	-	NC	125	126	VREFCA	-	
	-	Vss	127	128	Vss	-	
30	AL16	DQ32	129	130	DQ36	AL14	30
30	AJ16	DQ33	131	132	DQ37	AN15	30
	-	Vss	133	134	Vss	-	
30	AM15	DQS4#	135	136	DM4	AK16	30
30	AL15	DQS4	137	138	Vss	-	
	-	Vss	139	140	DQ38	AN14	30
30	AJ15	DQ34	141	142	DQ39	AP16	30
30	AK14	DQ35	143	144	Vss	-	
	-	Vss	145	146	DQ44	BA13	30
30	AY16	DQ40	147	148	DQ45	AW16	30
30	AY14	DQ41	149	150	Vss	-	
	-	Vss	151	152	DQS5#	BA15	30
30	AY17	DM5	153	154	DQS5	BA16	30
	-	Vss	155	156	Vss	-	
30	BA14	DQ42	157	158	DQ46	AW15	30
30	AY13	DQ43	159	160	DQ47	AV14	30
	-	Vss	161	162	Vss	-	

Bank No.	Pin No.	Signal Name	Pin No.		Signal Name	Pin No.	Bank No.
30	AU13	DQ48	163	164	DQ52	AT15	30
30	AV13	DQ49	165	166	DQ53	AT14	30
	-	Vss	167	168	Vss	-	
30	AR14	DQS6#	169	170	DM6	AR16	30
30	AP14	DQS6	171	172	Vss	-	
	-	Vss	173	174	DQ54	AT13	30
30	AU15	DQ50	175	176	DQ55	AT16	30
30	AV15	DQ51	177	178	Vss	-	
	-	Vss	179	180	DQ60	BB13	30
30	BB17	DQ56	181	182	DQ61	BC13	30
30	BC17	DQ57	183	184	Vss	-	
	-	Vss	185	186	DQS7#	BD14	30
30	BB16	DM7	187	188	DQS7	BD15	30
	-	Vss	189	190	Vss	-	
30	BD17	DQ58	191	192	DQ62	BC15	30
30	BD16	DQ59	193	194	DQ63	BC14	30
	-	Vss	195	196	Vss	-	
	-	SA0	197	198	EVENT#	-	
	-	VDDSPD	199	200	SDA		
	-	SA1	201	202	SCL		
	-	VTT	203	204	VTT	-	

7.5. PCI Express Edge Interface

The board allows a PCI Express x8 (8-Lane) Gen3 connection.

Table 7-9 PCI Express Edge Pinout Table

Bank No.	Pin No.	A		B	Pin No.	Bank No.
	1	PRSNT1_B	1	+V12	-	
	-	+V12	2	+V12	-	
	-	+V12	3	+V12	-	
		GND	4	GND		
	-	JTAG_TCK	5	SMCLK	-	
	-	JTAG_TDI	6	SMDAT	-	
	-	JTAG_TDO	7	GND		
	-	JTAG_TMS	8	+3.3V	-	
	-	+3.3V	9	JTAG_TRST#	-	
	-	+3.3V	10	+3.3VAUX	-	
BANK 17	H35	PERST#	11	WAKE#	-	
		GND	12	RESERVED	-	
Refer to the		REFCLK+	13	GND		
clock structure		REFCLK-	14	PETP0	AN6	MGTHRXP3_112
		GND	15	PETN0	AN5	MGTHRXN3_112
MGTHTXP3_112	AP4	PERP0	16	GND		
MGTHTXN3_112	AP3	PERN0	17	PRSNT2#	1	
		GND	18	GND		
	-	RESERVED	19	PETP1	AR6	MGTHRXP2_112
		GND	20	PETN1	AR5	MGTHRXN2_112
MGTHTXP2_112	AR2	PERP1	21	GND		
MGTHTXN2_112	AR1	PERN1	22	GND		
		GND	23	PETP2	AT4	MGTHRXP1_112
		GND	24	PETN2	AT3	MGTHRXN1_112
MGTHTXP1_112	AU2	PERP2	25	GND		
MGTHTXN1_112	AU1	PERN2	26	GND		
		GND	27	PETP3	AU6	MGTHRXP0_112
		GND	28	PETN3	AU5	MGTHRXN0_112
MGTHTXP0_112	AV4	PERP3	29	GND		
MGTHTXN0_112	AV3	PERN3	30	RESERVED	-	
		GND	31	PRSNT2#	1	
	-	RESERVED	32	GND		
	-	RESERVED	33	PETP4	AW6	MGTHRXP3_111
		GND	34	PETN4	AW5	MGTHRXN3_111
MGTHTXP3_111	AW2	PERP4	35	GND		
MGTHTXN3_111	AW1	PERN4	36	GND		
		GND	37	PETP5	AY4	MGTHRXP2_111
		GND	38	PETN5	AY3	MGTHRXN2_111
MGTHTXP2_111	BA2	PERP5	39	GND		
MGTHTXN2_111	BA1	PERN5	40	GND		

Bank No.	Pin No.	A		B	Pin No.	Bank No.
		GND	41	PETP6	BA6	MGTHRXP1_111
		GND	42	PETN6	BA5	MGTHRXN1_111
MGTHTXP1_111	BB4	PERP6	43	GND		
MGTHTXN1_111	BB3	PERN6	44	GND		
		GND	45	PETP7	BC6	MGTHRXP0_111
		GND	46	PETN7	BC5	MGTHRXN0_111
MGTHTXP0_111	BD4	PERP7	47	GND		
MGTHTXN0_111	BD3	PERN7	48	PRSNT2#	1	
		GND	49	GND		

The PCI Express lane width depends on the type of a resistor to be installed.
Table 7-10 shows PCI Express lane width configuration.

Table 7-10 PCI Express Lane Width Configuration

Device	Lane	Note
R470	x1	
R471	x4	
R472	x8	Default

The Clock(100MHz) from PCIexpress edge is buffered by IDT, ICS874003DGI-02(U42) then provide to FPGA.

ISC874003DGI-02(U42) has a Switch(SW4) for selecting clock frequesncy. But This board only targeting to PCIexpress interface. Please keep setting "All Off" to SW4.

7.6. PMOD Interface

The board provides a general PMOD interface.
The board has TI : TXS0108EPWR(U47) for signal level exchange purpose.
The PMOD connector (CN45) uses SAMTEC : SSW-106-01-F-D.

Table 7-11 PMOD Pinout Table

FPGA			TXS0108EPWR		Connector		
Pin No.	Bank	Level	Pin No.	Signal Name	Pin No.	Signal Name	Level
F34	17	1.8V	1	PMOD0	1	PMOD0_L	3.3V
E34	17		3	PMOD1	2	PMOD1_L	
A35	17		4	PMOD2	3	PMOD2_L	
A36	17		5	PMOD3	4	PMOD3_L	
					5	DGND	
					6	3.3V	
A33	17		6	PMOD4	7	PMOD4_L	
A34	17		7	PMOD5	8	PMOD5_L	
B36	17		8	PMOD6	9	PMOD6_L	
B37	17		9	PMOD7	10	PMOD7_L	
					11	DGND	
					12	3.3V	

7.7. QSPI-FLASH

The board has 1 x Micron : N25Q512A11G1240F(U54).

This QSFP Flash memory is using for user apploication. It is not connected to configuration pins.

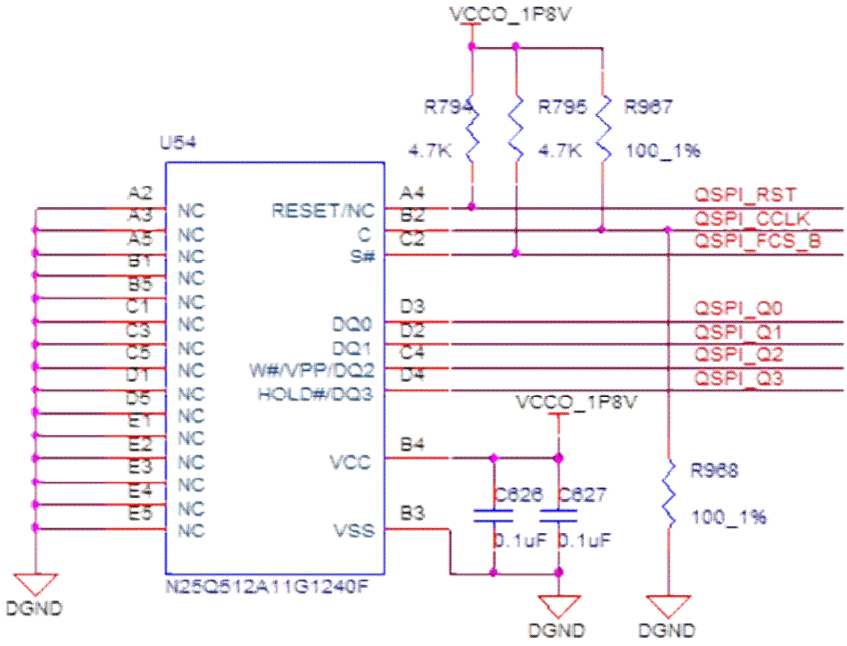

Figure 7-7 QSPI Layout

Table 7-12 QSPI Pinout Table

Device		FPGA		
Name	**Signal Name**	**Pin No.**	**Bank**	**Level**
A4	QSPI_RST	R34	15	1.8V
B2	QSPI_CCLK	L33	15	
C2	QSPI_FCS_B	U32	15	
D3	QSPI_Q0	L34	15	
D2	QSPI_Q1	M31	15	
C4	QSPI_Q2	M32	15	
D4	QSPI_Q3	N34	15	

7.8. USB3.0

This board has a CYUSB3014(U29) and USB3.0 TYPE-B connector(CN4).

Virtex-7 is connecting CYUSB3014 via Spartan3AN but Initial Spartan3AN design is supported USB3.0 bypass function.

Table 7-13 USB3.0 Pin Assign

Schematic	FPGA			
Signal Name	Pin No.	Bank	Level	Comment
USB_RESET	AU33	14		RESET_N
SP3_A23	M33	15		Slave FIFO clock
SP3_A17	R32	15		Slave FIFO chip select
SP3_A18	T33	15		Slave FIFO address[0]
SP3_A19	P31	15		Slave FIFO address[1]
SP3_A20	R31	15		Slave FIFO read enable
SP3_A21	T31	15		Slave FIFO output enable
SP3_A22	U31	15		Slave FIFO write enable
SP3_A16	R33	15		Slave FIFO Package End indication signal
SP3_D0	AN34	14		Slave FIFO data[0]
SP3_D1	AN35	14		Slave FIFO data[1]
SP3_D2	AJ34	14		Slave FIFO data[2]
SP3_D3	AK34	14		Slave FIFO data[3]
SP3_D4	AJ32	14		Slave FIFO data[4]
SP3_D5	AK32	14		Slave FIFO data[5]
SP3_D6	AL35	14		Slave FIFO data[6]
SP3_D7	AM35	14		Slave FIFO data[7]
SP3_D8	AL34	14		Slave FIFO data[8]
SP3_D9	AP32	14		Slave FIFO data[9]
SP3_D10	AR32	14		Slave FIFO data[10]
SP3_D11	AP34	14		Slave FIFO data[11]
SP3_D12	AP35	14	1.8V	Slave FIFO data[12]
SP3_D13	AT34	14		Slave FIFO data[13]
SP3_D14	AR33	14		Slave FIFO data[14]
SP3_D15	AR34	14		Slave FIFO data[15]
SP3_A00_D16	BD35	14		Slave FIFO data[16]
SP3_A01_D17	BD34	14		Slave FIFO data[17]
SP3_A02_D18	BD37	14		Slave FIFO data[18]
SP3_A03_D19	BD36	14		Slave FIFO data[19]
SP3_A04_D20	BC35	14		Slave FIFO data[20]
SP3_A05_D21	BC34	14		Slave FIFO data[21]
SP3_A06_D22	BC37	14		Slave FIFO data[22]
SP3_A07_D23	BC33	14		Slave FIFO data[23]
SP3_A08_D24	BB33	14		Slave FIFO data[24]
SP3_A09_D25	BB36	14		Slave FIFO data[25]
SP3_A10_D26	BB35	14		Slave FIFO data[26]
SP3_A11_D27	BA35	14		Slave FIFO data[27]
SP3_A12_D28	BA34	14		Slave FIFO data[28]
SP3_A13_D29	AY34	14		Slave FIFO data[29]
SP3_A14_D30	AW34	14		Slave FIFO data[30]
SP3_A15_D31	BA33	14		Slave FIFO data[31]
SP3_A24	N33	15		Slave FIFO(CMD channel) full/empty indication signal
SP3_A25	N32	15		Slave FIFO(Current channel) full/empty indication signal

7.9. LED

This board has 12 LEDs.

All these LEDs will be turned on when "High" is output from FPGA.

Figure 7-8 LED Layout

Table 7-14 LED Pinout Table

Device		FPGA		
Name	**Signal Name**	**Pin No.**	**Bank**	**Level**
LED0	LED0	AY26	11	1.5V
LED1	LED1	BA26	11	
LED2	LED2	BD24	11	
LED3	LED3	BD25	11	
LED4	LED4	BC25	11	
LED5	LED5	BD26	11	
LED6	LED6	BA25	11	
LED7	LED7	BB25	11	
LED8	LED8	BB26	11	
LED9	LED9	BB27	11	
LED10	LED10	BC27	11	
LED 11	LED 11	BD27	11	

7.10. GPIO Interface

The board has two 10 pin headers (CN34, CN35) and each connector has 8 signals that are connected to FPGA.(Total 16 signals)
The interface has FMC_VADJ (Default: 1.8V) voltage level.

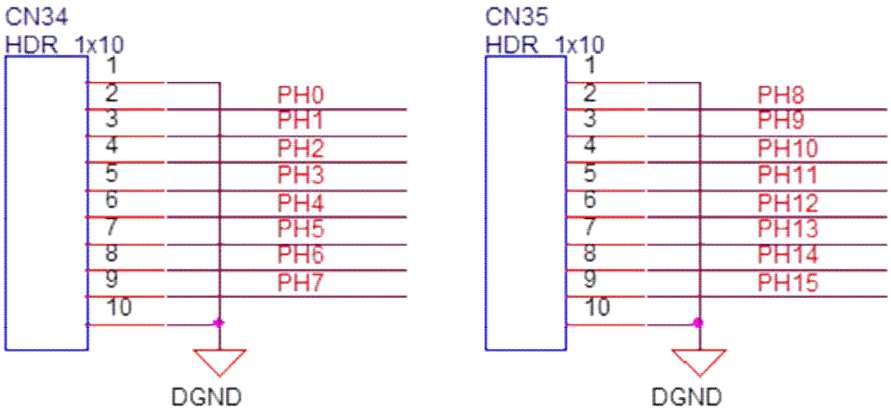

Figure 7-9 GPIO Pin Layout

Table 7-15 GPIO Pinout Table

FPGA		CN34		CN35		FPGA
Bank No.	Pin No.	Signal Name	Pin No.	Pin No.	Signal Name	Pin No.	Bank No.
	-	DGND	1	1	DGND	-	
16	V28	PH0	2	2	PH8	N30	16
16	U28	PH1	3	3	PH9	M30	16
16	R28	PH2	4	4	PH10	N28	16
16	R29	PH3	5	5	PH11	M28	16
16	U30	PH4	6	6	PH12	L29	16
16	T30	PH5	7	7	PH13	L30	16
16	P20	PH6	8	8	PH14	L28	16
16	N29	PH7	9	9	PH15	K28	16
	-	DGND	10	10	DGND	-	

7.11. DIPSW

The board has three 4 poles DIPSW (SW10, SW11, SW12).

When the DIPSW is set to the ON side, it generates "Low" on the associated FPGA pin.

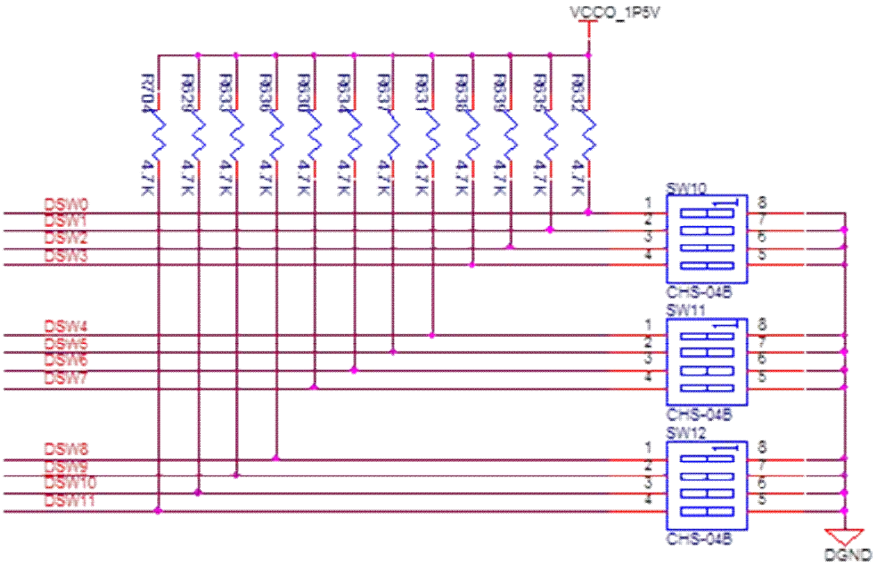

Figure 7-10 DIPSW Structure

Table 7-16 DIPSW Pinout Table

Device		FPGA		
Name	Signal Name	Pin No.	Bank	Level
SW10	DSW0	AY18	31	1.5V
	DSW1	BA18	31	
	DSW2	BB20	31	
	DSW3	BC20	31	
SW11	DSW4	BA20	31	
	DSW5	BA19	31	
	DSW6	BD21	31	
	DSW7	BD20	31	
SW12	DSW8	BB18	31	
	DSW9	BC18	31	
	DSW10	BC19	31	
	DSW11	BD19	31	

7.12. PUSHSW

The board has four PUSHSWs. When the PUSHSW is held down, it generates "Low" on the associated FPGA pin.

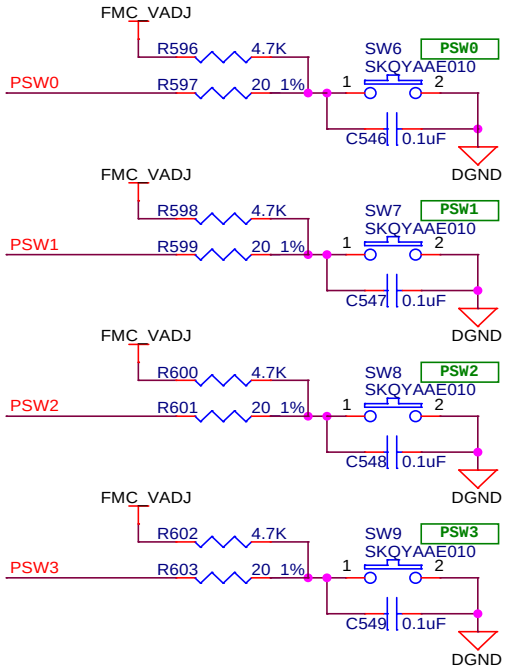

Figure 7-11 PUSHSW Structure

Table 7-17 PUSHSW Pinout

Device		FPGA		
Name	**Signal Name**	**Pin No.**	**Bank**	**Level**
SW6	PSW0	V29	16	FMC_VADJ(Default1.8V)
SW7	PSW1	V30	16	
SW8	PSW2	T28	16	
SW9	PSW3	T29	16	

7.13. Power Connector for FAN

This is a power supply connector for FAN.

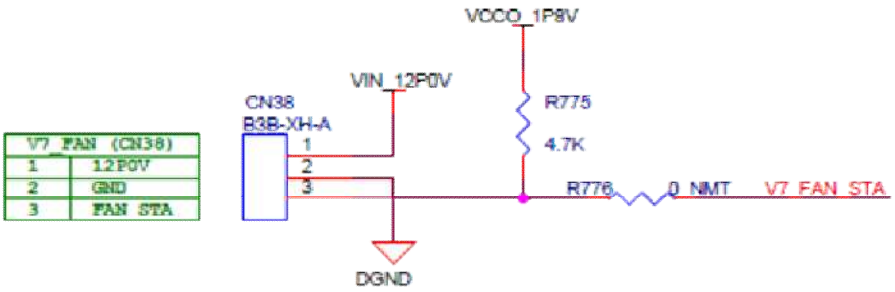

Figure 7-12 Power Connector for FAN

Table 7-18 External Power Supply Connector Pinout Table

Type	No.	1pin	2pin	3pin
Power Connector for FAN	CN38	12V	DGND	Sensor

7.14. Battery Control

The board has a battery control connector (CN8). It is not installed by default.

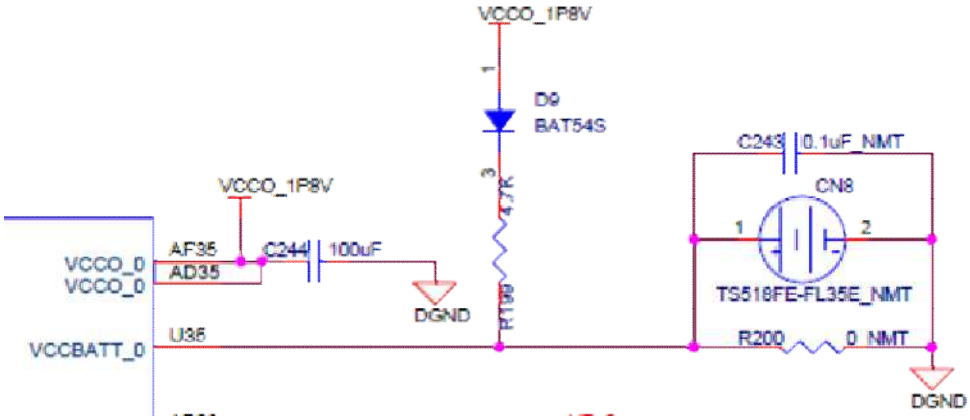

Figure 7-13 Battery

Table 7-19 Battery Control signal Pinout Table

Type	No.	1pin	2pin
Battery Input Connector	CN8	+ (1.0V to 2.5V)	- (GND)

7.15. XADC Pinheader

The board has a XADC pinheader connector (CN48).

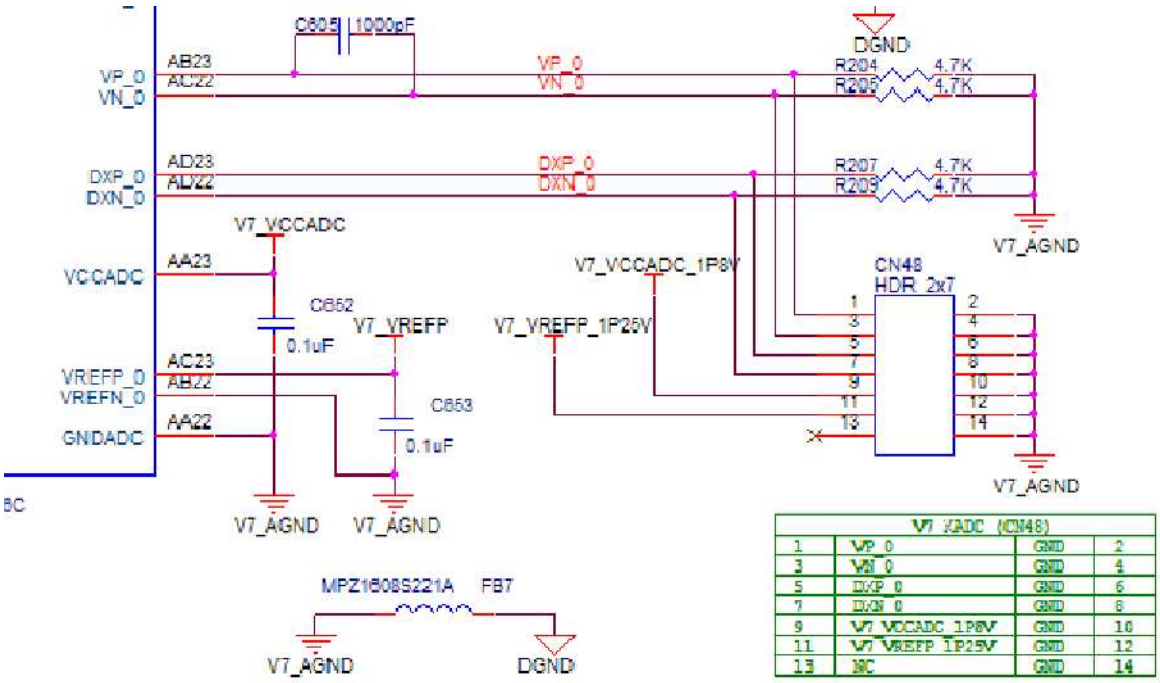

Figure 7-14 XADC Structure

Table 7-20 XADC Pinout Table

CN48		FPGA		
Name	**Signal Name**	**Pin No.**	**Bank**	**Level**
1	VP_0	AB23	0	1.8V
2	GND	-		
3	VN_0	AC22	0	
4	GND	-		
5	DXP_0	AD23	0	
6	GND	-		
7	DXN_0	AD22	0	
8	GND	-		
9	V7_VCCADC_1P8V	-		
10	GND	-		
11	V7_VREFP_1P25V	-		
12	GND	-		
13	NC	-		
14	GND	-		

8. Configuration

The board allows configuration using microSDCard and NandFlash.
Please see "uSD_CONF_UserManual_V7PCIEX_1_**e.pdf" for more detail of microSDCard configuration.

9. Initial Settings

This section describes initial settings for all Switch and CN(Jumper).

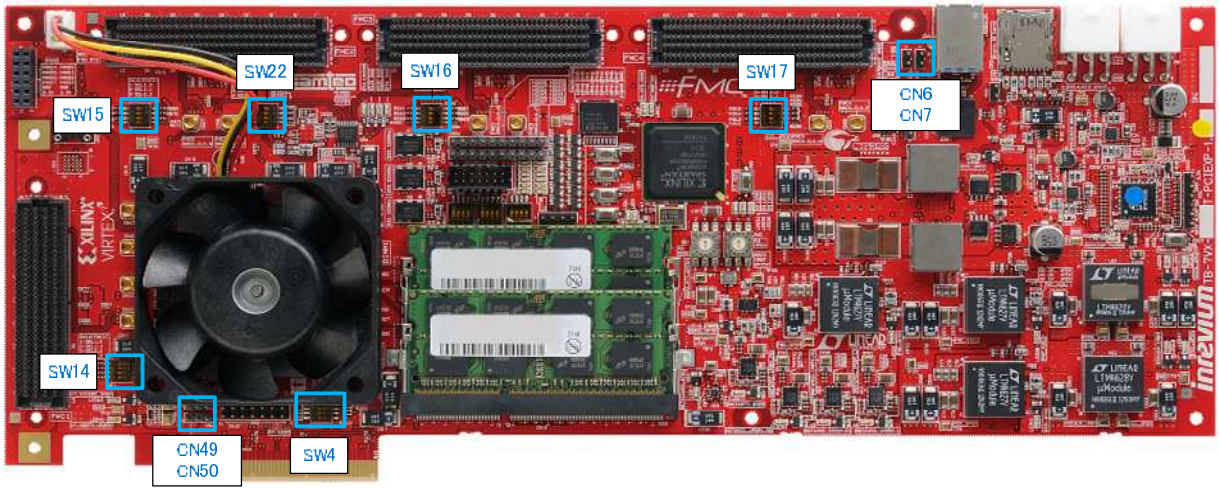

Figure 9-1 location of SW and CN(Juspmer)

Table 9-1 Initial Settings

No	Silk No.	Initial Setting	Function
1	SW4	ALL OFF	Selecting PCI-EXPRESS RefCLK
2	SW14	ALL OFF	Selecting FPGA FMC1 GTH RefCLK
3	SW15	ALL OFF	Selecting FPGA FMC2 GTH RefCLK
4	SW16	ALL OFF	Selecting FPGA FMC3 GTH RefCLK
5	SW17	ALL OFF	Selecting FPGA FMC4 GTH RefCLK
6	SW22	ALL OFF	Setting PLL
7	CN6	1-2	Setting USB BOOT MODE
8	CN7	1-2	Setting USB BOOT MODE
9	CN49	2-3	Selecting FPGA VREF
10	CN50	1-2	Selecting FPGA ACCADC

Please do not change CN6, CN7 CN49 and CN50.
Other CN(Jumper) are Non Connection setting.

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